MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

User's Manual

Terminal interface module type AJ71C21(S1)

CATALOG #JUM-198
$ 5.00

MITSUBISHI ELECTRIC

REVISIONS

※The manual number is given on the bottom left of the back cover.

Print Date	Manual Number	Revision
Jul., 1989	IB (NA) 66198-A	First edition

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

1. GENERAL DESCRIPTION
2. SYSTEM CONFIGURATION
3. SPECIFICATIONS
4. SETTINGS AND PROCEDURES REQUIRED FOR OPERATION
5. BASIC PROGRAM MODE
6. SEQUENCE PROGRAM MODE
7. TROUBLESHOOTING
APPENDICES

CONTENTS

1. GENERAL DESCRIPTION ..... 1-1 ~ 1-2

1.1 Features 1-2

2. SYSTEM CONFIGURATION ..... 2-1 ~ 2-11

2.1 Overall Configuration 2-1
2.2 Application Systems 2-4
2.3 Example of System Configuration with the A3MCPU 2-5
2.3.1 BASIC program mode 2-5
2.3.2 Sequence program mode 2-7
2.3.3 BASIC program mode and Sequence program mode 2-8
2.4 Example of System Configuration with PC CPU 2-9
2.5 Components 2-10

3. SPECIFICATIONS ..... 3-1 ~ 3-10

3.1 General Specifications 3-1
3.2 Performance Specifications 3-2
3.3 Specifications 3-3
3.3.1 RS-232C connector specifications 3-3
3.3.2 RS-422 connector specifications 3-6
3.4 Function List 3-7
3.5 I/O for PC CPU 3-8
3.6 Buffer Memory 3-10

4. SETTINGS AND PROCEDURES REQUIRED FOR OPERATION ..... 4-1 ~ 4-14

4.1 Settings and Procedures Required for Operation 4-1
4.2 Handling Precautions 4-2
4.3 Nomenclature 4-3
4.3.1 Nomenclature 4-3
4.3.2 LED display 4-4
4.4 Switch Settings 4-5
4.4.1 I/F mode setting 4-5
4.4.2 Program mode and RS-232C/RS-422 terminal settings 4-7
4.4.3 RS-232C/RS-422 communication mode setting 4-8
4.5 Test Mode 4-9
4.5.1 Individual station loopback test 4-9
4.5.2 RAM check 4-11
4.6 Wiring Connections 4-12
4.6.1 Wiring precautions 4-12
4.6.2 RS-232C connector connections 4-12
4.6.3 RS-422 connections 4-13
4.7 Inspection and Maintenance 4-14
4.7.1 Battery replacement (for the AJ71C21-S1 only) 4-14

5. BASIC PROGRAM MODE ····· 5-1 ~ 5-3

5.1 The BASIC Console ····· 5-1
5.2 General-Purpose Port ····· 5-1
5.3 File I/O (for the AJ71C21-S1 only) ····· 5-2

6. SEQUENCE PROGRAM MODE ····· 6-1 ~ 6-28

6.1 Communication with External Equipment in the No Protocol Mode ····· 6-1
6.1.1 Basics in no protocol mode ····· 6-1
6.1.2 Buffer memory ····· 6-2
6.1.3 Program creation precautions ····· 6-4
6.1.4 Handshake I/O signals ····· 6-4
6.1.5 Error LED display status read ····· 6-5
6.1.6 Error LED off ····· 6-6
6.1.7 Word/byte specification ····· 6-7
6.1.8 Send buffer memory area setting ····· 6-8
6.1.9 Receive buffer memory area setting ····· 6-9
6.1.10 Receive end data number (fixed length) setting ····· 6-10
6.1.11 Receive end code setting ····· 6-11
6.1.12 Send in no protocol mode (AJ71C21 → computer) ····· 6-12
6.1.13 Receive in no protocol mode (external equipment → AJ71C21) ····· 6-15
6.2 Data Read/Write (Only for the AJ71C21-S1) ····· 6-21
6.2.1 Data read/write ····· 6-21
6.2.2 I/O handshake signals ····· 6-22
6.2.3 RAM write ····· 6-23
6.2.4 RAM read ····· 6-25
6.2.5 RAM error read and clear ····· 6-27
6.2.6 Memory data backup ····· 6-27

7. TROUBLESHOOTING ····· 7-1 ~ 7-8

7.1 Troubleshooting in BASIC Program Mode ····· 7-1
7.1.1 Troubleshooting flowchart ····· 7-1
7.1.2 CRT display faulty ····· 7-2
7.2 Troubleshooting in Sequence Program Mode ····· 7-3
7.2.1 Troubleshooting during communication with external equipment in no protocol mode ····· 7-3
7.2.2 RAM write/read error ····· 7-8

APPENDICES ····· APP-1 ~ APP-4

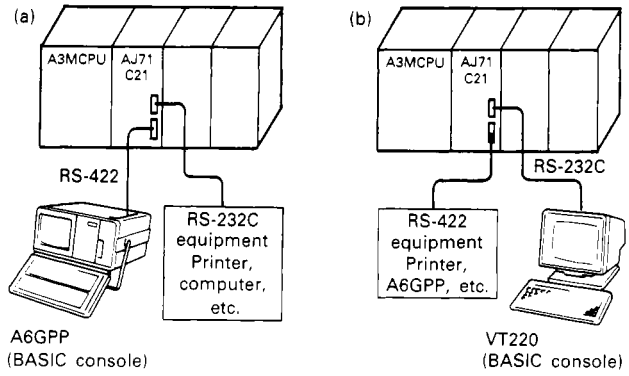
APPENDIX 1 Comparison in Function between the AJ71C21 and the AJ71C24-S3 (Computer Link Module) ····· APP-1
APPENDIX 2 ASCII Code Table ····· APP-2
APPENDIX 3 Display Control Code List ····· APP-3
APPENDIX 4 Dimensions ····· APP-4

1. GENERAL DESCRIPTION

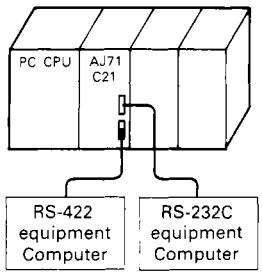
This manual describes the specifications and handling of the AJ71C21 terminal interface module and the AJ71C21-S1 terminal interface module (hereafter referred to as the AJ71C21).
As a modified version of the AJ71C21, the AJ71C21-S1 features an added built-in RAM memory of 320 Kbytes. The AJ71C21 is designed to be connected to RS-232C or RS-422 device. It can be used in one of two modes : the BASIC program mode which matches the A3MCPU BASIC functions and the sequence program mode in which it is compatible with the PC CPU.

Connection Examples

1. BASIC program mode
   (1) Used as BASIC console interface



2. Sequence program mode
   Used as computer link interface without protocol



The term "PC CPU" refers to the following types of PC CPUs.
The term "A6GPP" refers to the A6GPP/A6HGP/A6PHP.

A0J2CPU(P23/R23)	
A1NCPU(P21/R21)	A1(E)CPU(P21/R21)
A2NCPU(P21/R21)	A2(E)CPU(P21/R21)
A3NCPU(P21/R21)	A3(E)CPU(P21/R21)
A3MCPU(P21/R21)	A3HCPU(P21/R21)

1.1 Features

The AJ71C21 has the following advantages when used in the BASIC program mode and the sequence program mode.

(1) In the BASIC program mode
The AJ71C21 is used to perform the BASIC functions of the A3MCPU.
1) I/F for connection with BASIC console
This interface offers the capability of BASIC program development and data I/O through the connected GPP/VT220.
2) Ports are provided for RS-232C and RS-422. As a general-purpose port, the AJ71C21 can be connected with the RS-232C or RS-422.
3) Since the built-in RAM can be used as a file memory, the AJ71C21-S1 lends itself to file management based on the BASIC.

(2) In the sequence program mode
This mode meets the requirements of the conventional PC CPU.
1) When in the no protocol mode (as with the AJ71C24-S3 computer link module), communication can be established with external equipment.
2) The built-in RAM contained in the AJ71C21-S1 can be used as a large-capacity memory for storing data.

IB (NA) 66198-A

2. SYSTEM CONFIGURATION

This chapter describes system configurations which may be combined with the AJ71C21.

2.1 Overall Configuration

Fig. 2.1 and Fig. 2.2 shows the overall configuration of A series system which is loaded with the AJ71C21.

(1) Building block type CPU

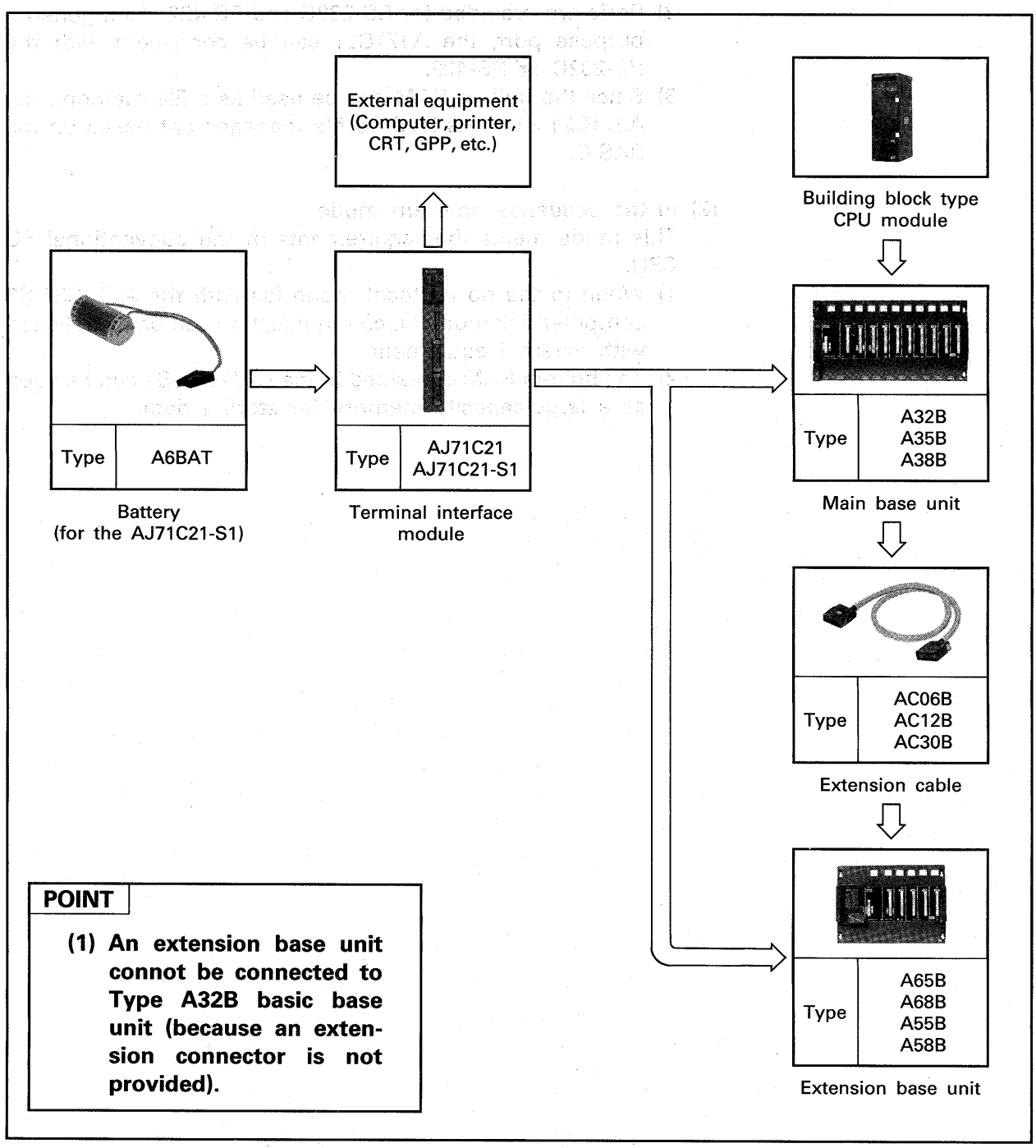


Fig. 2.1 Overall Configuration of Building Block Type CPU

(2) Compact type CPU

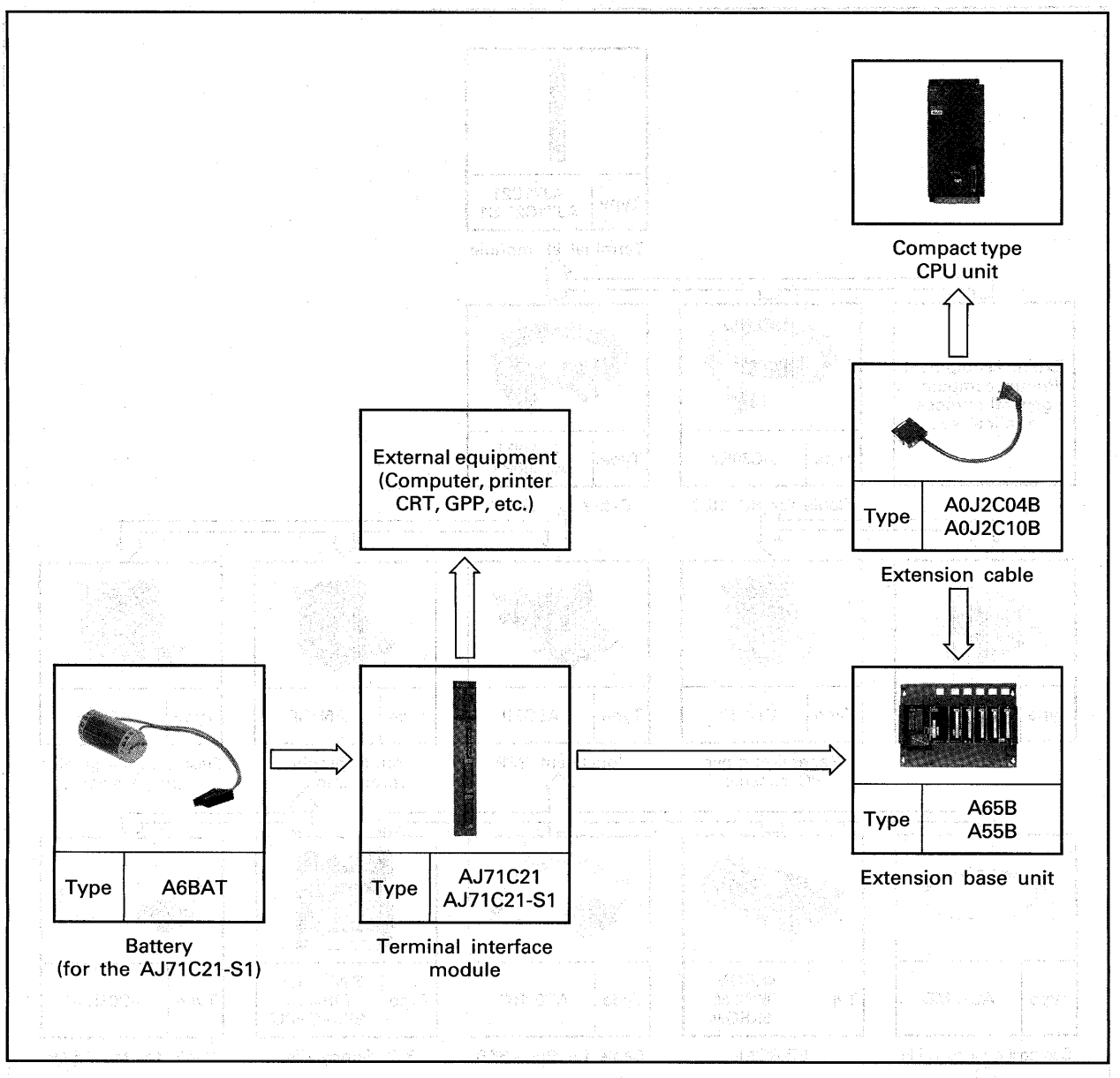


Fig. 2.2 Overall Configuration of Compact Type CPU

(3) Peripheral equipment configuration

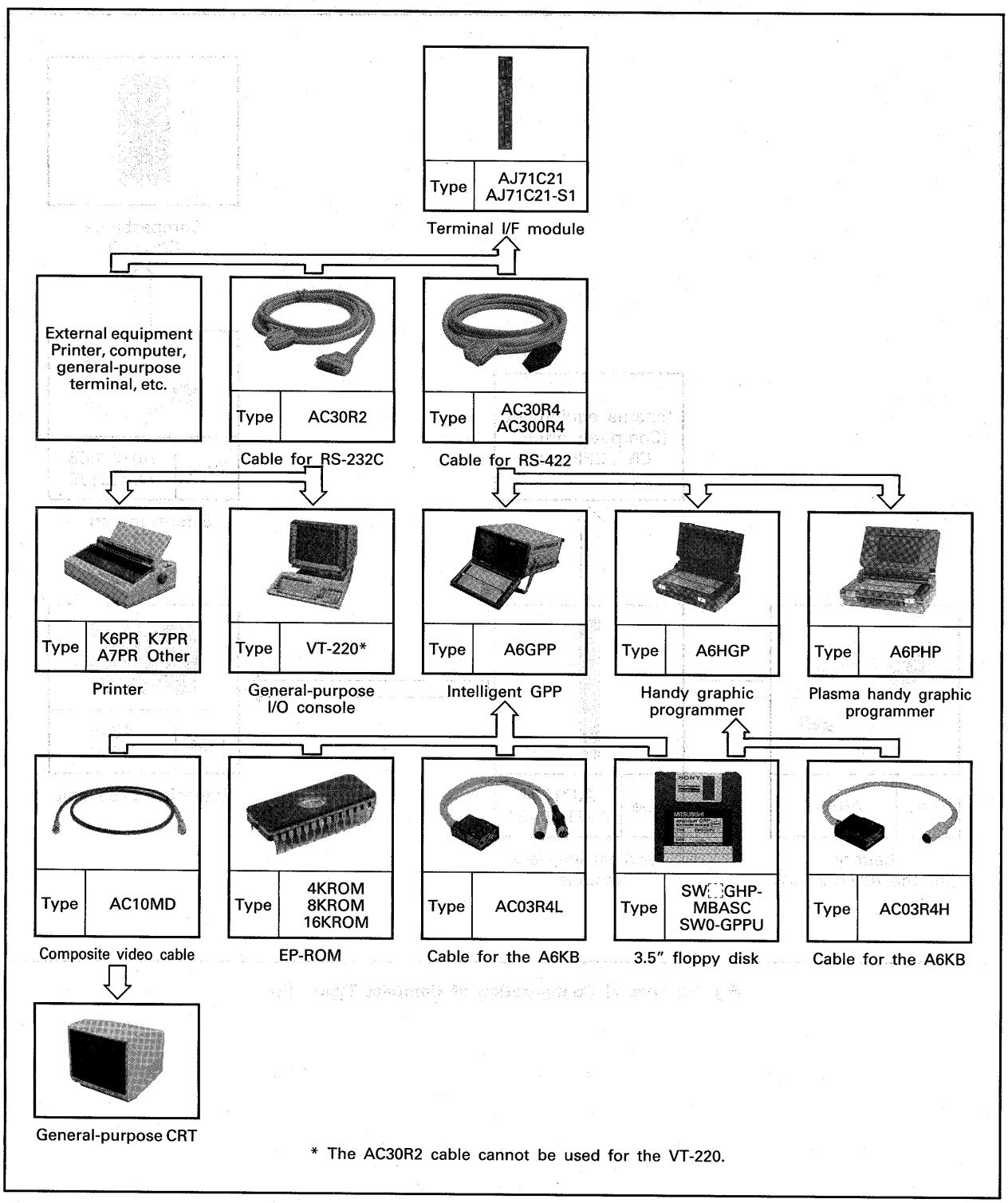


Fig. 2.3 Peripheral Equipment Configuration

POINT

The GPP/HGP/PHP consoles and the general-purpose I/O console (VT-220) are selected with the DIP switch. For details, refer to Section 4.4.1.

2.2 Application Systems

The CPU applicable to the AJ71C21 varies with the application. Table 2.1 lists the applicable CPUs and describes restrictions on their use.

(1) Applicable system

Mode	BASIC Program Mode	Sequence Program Mode	
Applicable CPU	A3MCPU	A0J2CPU A1NCPU A2NCPU A3NCPU A3MCPU	 A1(E)CPU A2(E)CPU A3(E)CPU A3HCPU
MELSECNET data link system (1) CPU applicable to master station	A3MCPUP21/R21	A1NCPUP21/R21 A2NCPUP21/R21 A3NCPUP21/R21 A3MCPUP21/R21	A1(E)CPUP21/R21 A2(E)CPUP21/R21 A3(E)CPUP21/R21 A3HCPUP21/R21
(2) CPU applicable to local station	A3MCPUP21/R21	A0J2CPUP23/23 A1NCPUP21/R21 A2NCPUP21/R21 A3MCPUP21/R21	 A1(E)CPUP21/R21 A2(E)CPUP21/R21 A3(E)CPUP21/R21 A3HCPUP21/R21
Restrictions on Use (1) Number of interfaces used	Up to 2 interfaces can be used for each PC CPU.*1	Any number of interfaces can be used.	
(2) Loading slot*2	Interfaces can be loaded into any desired slot in the main base unit and extension base unit	Interfaces cannot be loaded into the last slot in the 7th extension stage of the A3CPU.	

Table 2.1 Applicable System

*1 When the AJ71C21 is used with the following modules, up to 2 interfaces, including the one used, can be used in each.
AJ71C24(S3) computer link module
AD51(S3) intelligent communication module
AJ71C22 multidrop link system module
AJ71C23 master controller high-speed link module

*2 The AJ71C21 cannot be loaded on the remote I/O station.

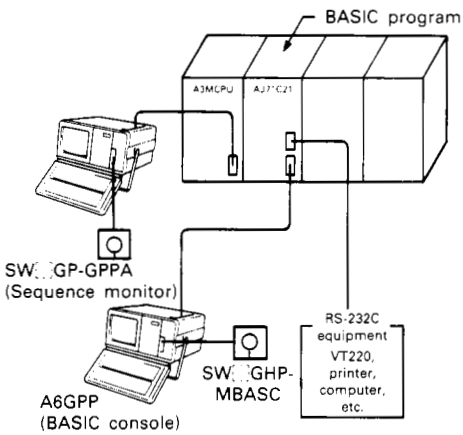
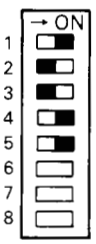
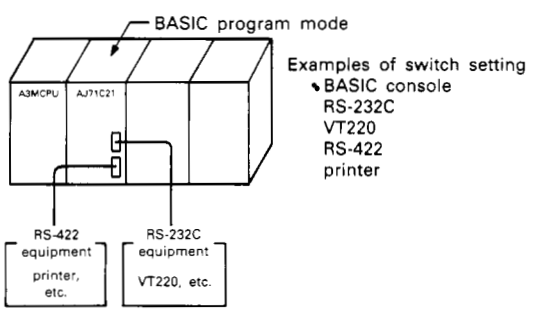
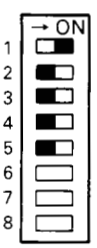
(2) The use of single AJ71C21 in both the BASIC and sequence modes is not allowed.

(3) The AJ71C21 I/F port is not intended for multidrop. Use the interface in format 1 : 1.

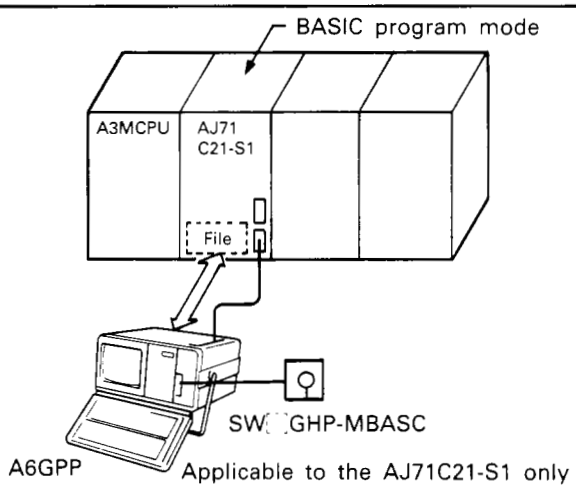
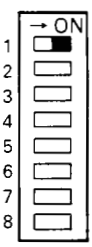
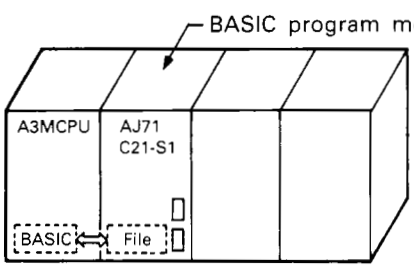
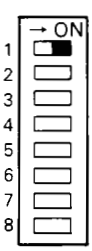
IB(NA)66198-A

2.3 Example of System Configuration with the A3MCPU

2.3.1 BASIC program mode

Method of Use	System Configuration	Switch Setting: Mode selection	Switch Setting: Program mode setting terminal
A6GPP used as BASIC console			
RS-232C/RS-422 used as a general-purpose port			

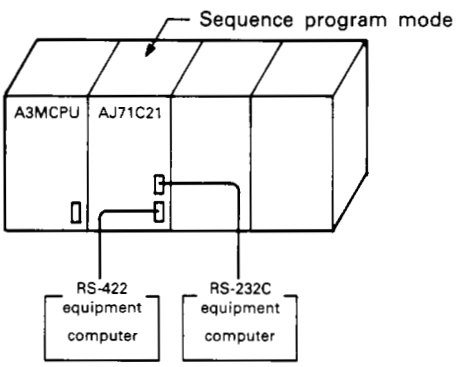
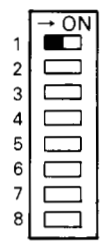
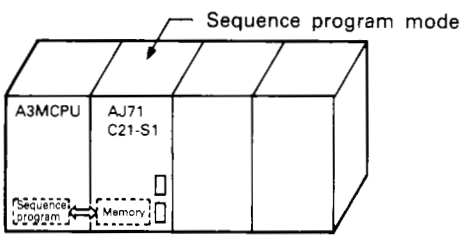
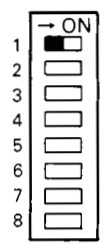
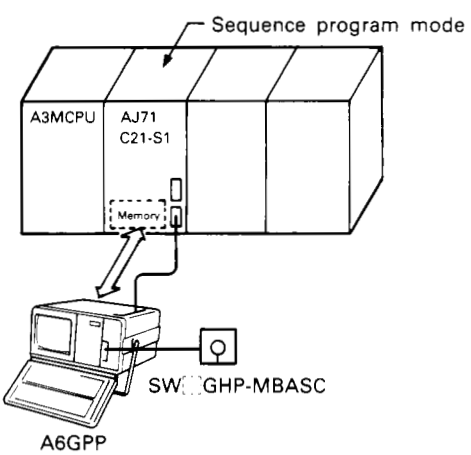
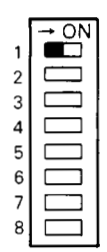
For details on switch setting, refer to Section 4.4.

Method of Use	System Configuration	Switch Setting	
		Mode selection	Program mode setting terminal
File access from the A6GPP	 Applicable to the AJ71C21-S1 only		
File access from BASIC	 Applicable to the AJ71C21-S1 only	Modes 0, 1, and 2 can be set.	

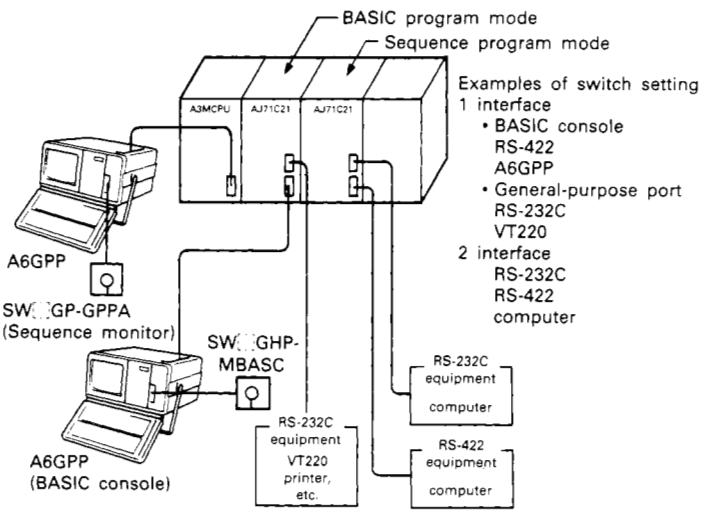
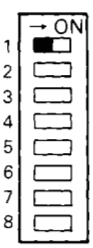
2

IB (NA) 66198-A

2.3.2 Sequence program mode

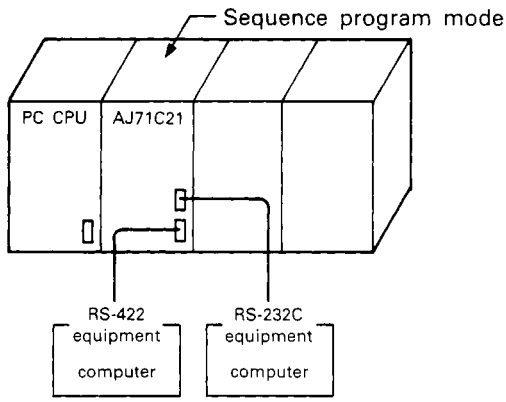
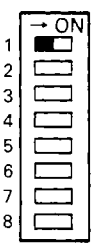
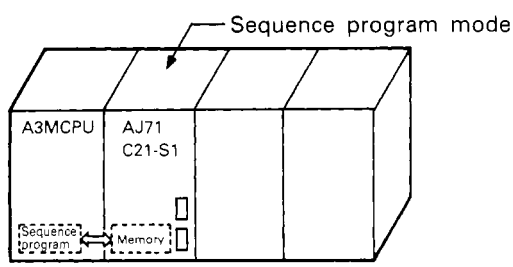
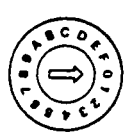
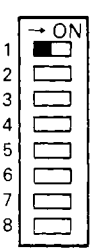
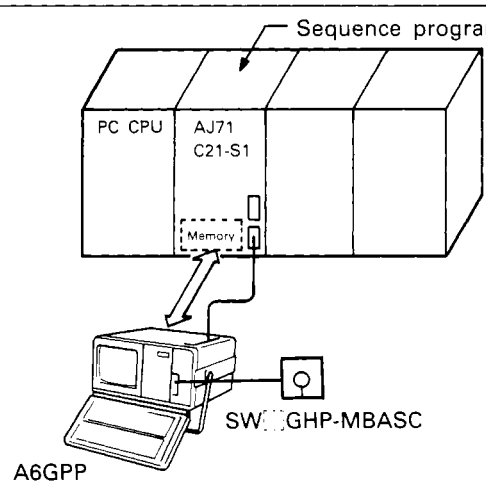
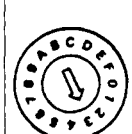
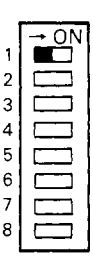
Method of Use	System Configuration	Switch Setting	
		Mode selection	Program mode setting terminal
Communication via RS-232C/RS-422 without protocol			
Data write to and read from the memory	 Applicable to the AJ71C21-S1 only		
Memory backup	 Applicable to the AJ71C21-S1 only		

2.3.3 BASIC program mode and Sequence program mode

Method of Use	System Configuration	Switch Setting	
		Mode selection	Program mode setting terminal
1 interface A6GPP used as BASIC console 2 interfaces Communication via RS-232C/ RS-422 without protocol			

2

2.4 Example of System Configuration with PC CPU

Method of Use	System Configuration	Switch Setting: Mode selection	Switch Setting: Program mode setting terminal
Communication via RS-232C/RS-422 without protocol			
Data write to and read from the memory	 Applicable to the AJ71C21-S1 only		
Memory backup	 Applicable to the AJ71C21-S1 only		

2.5 Components

For details on the components, refer to their individual User's Manual.

<table>
<tr><th rowspan="2">Component</th><th rowspan="2">Type</th><th rowspan="2">Remarks</th><th colspan="2">Applicable System</th></tr>
<tr><th>Basic program mode</th><th>Sequence program mode</th></tr>
<tr><td rowspan="2">AJ71C21 terminal interface module</td><td>AJ71C21</td><td>Main module</td><td>○</td><td>○</td></tr>
<tr><td>AJ71C21-S1</td><td>Main modulh, RAM320K (Battery back-up)</td><td>○</td><td>○</td></tr>
<tr><td>Battery</td><td>A6BAT</td><td>For ICRAM (for AJ71C21-S1)</td><td>○</td><td>○</td></tr>
<tr><td>Intelligent GPP</td><td>A6GPPE-SET</td><td>This GPP consists of the following.
<table>
<tr><th>Type</th><th>Remarks</th></tr>
<tr><td>A6GPPE</td><td>• Programming equipment with CRT
• Provided with ROM writer function, FDD function, and printer interface function</td></tr>
<tr><td>SW□GP-GPPAEE/EG</td><td>System FD for the A series</td></tr>
<tr><td>SW□GP-GPPKEE/EG</td><td>System FD for the K series</td></tr>
<tr><td>SW□-GPPU</td><td>FD for user program storage (3.5"; formatted)</td></tr>
<tr><td>AC30R4</td><td>Cable connecting the AJ71C21 module with the A6GPP, 3m (11.8inch)</td></tr>
</table></td><td>○</td><td>○</td></tr>
<tr><td>Handy graphic programmer</td><td>A6HGPE-SET</td><td>This GPP consists of the following.
<table>
<tr><th>Type</th><th>Remarks</th></tr>
<tr><td>A6HGPE</td><td>• Programming equipment with LCD
• Provided with ROM writer function, FDD function, and printer interface function</td></tr>
<tr><td>SW□-HGPAEE/EG</td><td>System FD for the A series</td></tr>
<tr><td>SW□-HGPKEE/EG</td><td>System FD for the K series</td></tr>
<tr><td>SW□-GPPU</td><td>FD for user program storage (3.5"; formatted)</td></tr>
<tr><td>AC30R4</td><td>Cable connecting the AJ71C21 module with the A6GPP, 3m (11.8inch)</td></tr>
</table></td><td>○</td><td>○</td></tr>
<tr><td>Plasma handy graphic programmer</td><td>A6PHPE-SET</td><td>This GPP consists of the following.
<table>
<tr><th>Type</th><th>Remarks</th></tr>
<tr><td>A6PHPE</td><td>• Programming equipment with plasma display
• Provided with ROM writer function, FDD function, and printer interface function</td></tr>
<tr><td>SW□GP-GPPAEE/EG</td><td>System FD for the A series</td></tr>
<tr><td>SW□GP-GPPKEE/EG</td><td>System FD for the K series</td></tr>
<tr><td>SW□-GPPU</td><td>FD for user program storage (3.5"; formatted)</td></tr>
<tr><td>AC30R4</td><td>Cable connecting the AJ71C21 module with the A6GPP, 3m (11.8inch)</td></tr>
</table></td><td>○</td><td>○</td></tr>
<tr><td>Software package for system startup</td><td>SW□GHP-MBASC</td><td>Software package for system startup required for use of the GPP/HGP/PHP as an AJ71C21 I/O console</td><td>○</td><td>○</td></tr>
<tr><td>User FD</td><td>SW0-GPPU</td><td>FD for storing user program (formatted)</td><td>○</td><td>○</td></tr>
<tr><td>Composite video cable</td><td>AC10MD</td><td>Connecting cable for monitoring GPP screen data, 1m (3.94inch)</td><td>○</td><td>○</td></tr>
<tr><td>General-purpose I/O console</td><td>VT-220
VT-100</td><td>Consoles complying with the display control code for the DEC VT-220 or equivalent can be used.</td><td>○</td><td></td></tr>
</table>

Table 2.2 lists the components required for use with the AJ71C21

IB (NA) 66198 A

Component	Type	Remarks	Applicable System	
			Basic program mode	Sequence program mode
Printer	K6PRE K7PRE	For program list and data	○	○
Cable for RS-422	AC30R4	Cable connecting the AJ71C21 module with the A6GPP, 3m (11.8inch)	○	○
Cable for RS-232C	AC30R2	Cable required when the AJ71C21 and printer (K6PRE, K7PRE) and the DEC VT-220 are used as consoles, 3m (11.8inch).	○	○

REMARKS

For the specifications of the general-purpose CRT connected to the A6GPP, refer to the A6GPP User's Manual.

IB (NA) 66198-A

3. SPECIFICATIONS

3.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55°C				
Storage ambient temperature	−20 to 75°C				
Operating ambient humidity	10 to 90%RH, no condensation				
Storage ambient humidity	10 to 90%RH, no condensation				
Vibration resistance	Conforms to *JIS C 0911	**Frequency**	**Acceleration**	**Amplitude**	**Sweep Count**
		10 to 55Hz	—	0.075mm (0.003inch)	10 times
		55 to 150Hz	1g	—	*(1 octave/minute)
Shock resistance	Conforms to JIS C 0912 (10g × 3 times in 3 directions)				
Noise durability	By noise simulator 1500Vpp noise voltage, 1 μs noise width and 25 to 60Hz noise frequency				
Dielectric withstand voltage	500V AC for 1 minute across batch of DC external terminals and ground				
Insulation resistance	50MΩ or more with 500V DC insulation resistance tester at the same location as dielectric strength.				
Operating ambience	No corrosive gases or dust.				
Cooling method	Self-cooling				

Table 3.1 General Specifications

REMARKS

(1) One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

(2) The noise durability and dielectric withstand voltage indicated above are as measured without the RC-232C or RS-422 interface.

*JIS: Japanese Industrial Standard

3.2 Performance Specifications

The AJ71C21 performance specifications are indicated in Table 3.2.

Item				Specifications	
				AJ71C21	AJ71C21-S1
Interfafe		RS-422 I/F		EIA. RS-422	
		RS-232C I/F		EIA. RS-232C	
Built-in RAM				Not provided	Provided
Storage capacity	BASIC program mode		Unformatted		320 KB
			Formatted	-	307 KB
			Number of files	-	256
	Sequence progrom mode				320 KB
Battery backup				Not provided	Provided
Battery specifications				-	Lithium battery for built-in battery backup (A6BAT) Cumulative power failure compensation period, 29 days Battery life, 5 years
Number of I/O occupied points				32	
Internal current consumption				5V DC 0.8A	5V DC 0.9A
Weight kg (lb)				0.4 (0.88)	0.5 (1.1)
External dimensions mm (inch)				250(9.84)×37.5(1.48)×120(4.72)	

Table 3.2 Performance Specifications

IB (NA) 66798-A

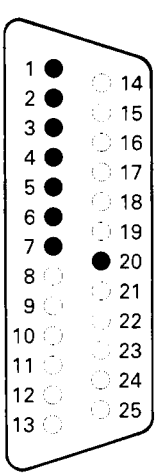
3.3 Specifications

This section describes the AJ71C21's built-in RS-232C and RS-232C.

3.3.1 RS-232C connector specifications

Item	Specifications
Connected equipment	Computer, personal computer, printer, modem, etc., designed for connection with the RS-232C interface
Transmission system	Full duplex communication system conforming to the EIA. RS-232C
Transmission speed (BPS)	Able to select 600, 1200, 2400, 4800, 9600, and 19200
Synchronous system	Asynchronous system
USART mode selection	Baud rate setting (able to select 600, 1200, 2400, 4800, 9600, and 19200 BPS) Parity bit setting — With parity / Without parity — Even parity / Odd parity Stop bit setting — Stop bit 1 / Stop bit 2 Character data bit setting — Data 7 bits / Data 8 bits Communication control setting — X_{ON}/X_{OFF} control / Control via DTR terminal

Connector specifications



Pin Number	Name	Signal Abbreviation	Signal Direction AJ71C24↔ Computer
1	Frame ground	FG	←→
2	Send data	SD (TXD)	→
3	Receive data	RD (RXD)	←
4	Requenst to sent	RS (RTS)	→
5	Clear to send	CS (CTS)	←
6	Data set ready	DSR (DR)	←
7	Signal ground	SG	←→
20	Data terminal ready	DTR (ER)	→

Table 3.3 RS-232C Interface Specifications

(1) Signals are described below.

FG : Frame ground. Connect the cable screening to pin 1 of the AJ71C21. When FG terminals are provided on both the computer and the AJ71C21, connect the screening to either of the FG terminals.
If the screening is connected to both FG terminals, data may not be properly transmitted due to noise or other factors.

RS : Turns on when the AJ71C21 hardware is ready. Remains on during data transmission.

CS : Data is not transmitted from the AJ71C21 when this signal turns off.
Therefore, CS should always be on.

DSR : Data is not transmitted from the AJ71C21 when this signal turns off. Send the signal from the computer so that DSR always is on.

DTR : Turns on when the AJ71C21 is ready to receive data.

(2) ON/OFF definitions are as follows:
ON : 5V to 15V DC
OFF : −5V to −15V DC

(3) Connector for interface
Use a mating connector that matches the RS-232C/RS-422 connector of the following type.
25-Pin D-sub (female) screw fixing type

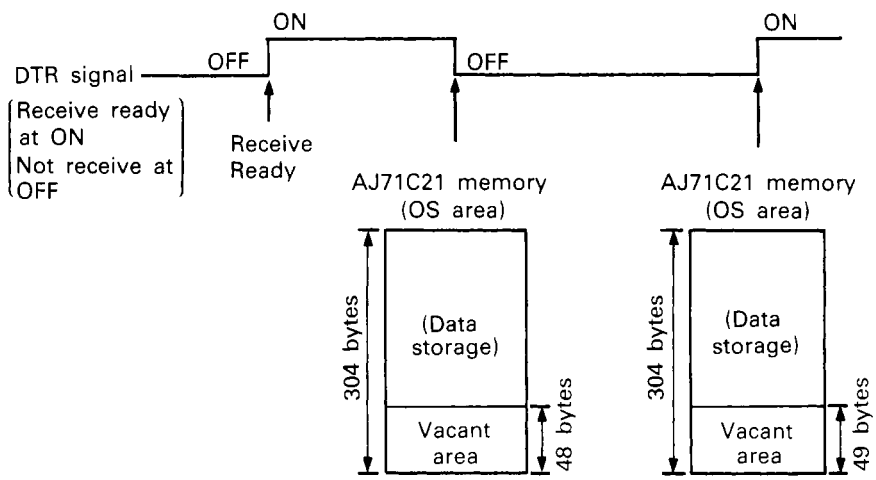
POINT

In some external equipment (such as a printer), the FG pin is connected to the SG pin. When connection such equipment, do not connect pin 1 of the AJ71C21 RS-232C connector.

IB (NA) 66198-A

(4) DTR, X_{ON}/X_{OFF} control
The data storage area of the AJ71C21 has a 304 byte capacity. It is used to turn on and off the DTR signal or send XON or XOFF.

	DTR signal	X_{ON}/X_{OFF}
• Vacant storage area has 48 bytes capacity or less.	···OFF	X_{OFF} transmission
• Vacant storage area has 49 bytes capacity or more.	···ON	X_{ON} transmission

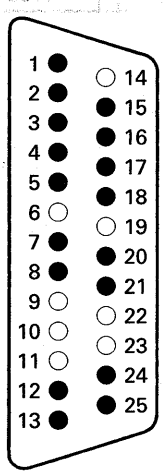


3

3.3.2 RS-422 connector specifications

Item	Specifications
Connected equipment	A6GPP, printer, personal computer, etc.,
Transmission system	Full duplex communication system conforming to the EIA. RS-422
Synchronous system	Asynchronous system
USART mode selection	Baud rate setting (able to select 600, 1200, 2400, 4800, 9600, and 19200 BPS) Parity bit setting — With parity / Without parity — Even parity / Odd parity Stop bit setting — Stop bit 1 / Stop bit 2 Character data bit setting — Data 7 bits / Data 8 bits Communication control setting — X_{ON}/X_{OFF} control / Control via DTR terminal

Connector specifications



Signal Designation		Block Diagram	Pin	Signal Direction	Remarks
Send data	SDA	(+) (−)	③	→External equipment	
	SDB		⑯		
Receive data	RDA	(+) 330 (−)	②	←External equipment	
	RDB		⑮		
Terminal ready notice	CSA	(+) (−)	⑤	→External equipment	
	CSB		⑱		
Data equipment ready	RSA	(+) 330 (−)	④	←External equipment	
	RSB		⑰		
DC current			⑫ ⑬ ㉔ ㉕		Do not make wiring connections.
Signal ground	SGA		⑦ ⑧ ⑳		Inside connected equipment
	SGB		㉑		
Frame ground	FG		①		

*: Connect pin 21 to the signal ground of the connected equipment.

Table 3.4 RS-422 Interface Specifications

3.4 Function List

Table 3.5 lists the functions performed by the AJ71C21.

Mode	Function	Description	Model Connected		I/F Mode Setting		Refer to:
					Online	Offline	
BASIC program mode	Console for BASIC	Used as a console for the A3MCPU's BASIC functions	RS-422	A6GPP (SW□GHP-MBASC)	○		Section 5.1
			RS-232C	VT-220			
	File I/O *2	The built-in file can be used as an extension file memory. This means that file management including the BASIC-based SAVE, LOAD, and other functions can be accomplished.	A3M		○		Section 5.3
			A6GPP (SW□GHP-MBASC)			○	
	General-purpose port	In response to the BASIC instruction, data can be input and output via the general-purpose port connected to the AJ71C21 RS-232C or RS-422.	RS-422	A6GPP printer	○		Section 5.2
			RS-232C	VT220 printer computer			
Sequence program mode	No protocol communication	Communication with the PC CPU and external equipment (general-purpose computer, printer, etc.) is done without protocol. *1	RS-422	General-purpose computer, printer, etc.	○		Section 6.1
			RS-232C				
	Data read/write *2	The built-in RAM can be used as a large-capacity memory. The PC CPU writes data to and reads data to and from this memory space.	Programmble Controller CPU		○		Section 6.2
			A6GPP (SW□GHP-MBASC)			○	

Table 3.5 AJ71C21 Function List

*1 The RS-232C and RS-422 are capable of receiving data simultaneously. However, processing through the RS-422 may be delayed if data communication is continuously and simultaneously performed through the RS-232C and RS-422 at a baud rate of 19200 bps.

*2 This function is effective only in the case of the AJ71C21-S1 (with a built-in 320K byte RAM).
For details on the I/F mode, refer to Section 4.4.1.

3.5. I/O for PC CPU

I/O signals for the PC CPU of the AJ71C21 are as indicated below. The number (n) suffixed to X or Y varies with the installation position of this module.

(1) Input signals (AJ71C21→PC CPU)
Input signals number 16: X_n0 through X_nF.

Input Signal	Signal Designation		Description	BASIC Program Mode	Sequence Program Mode
X_n0	Watch dog timer error		Turns on when watch dog timer error occurs in AJ71C21.	○	○
X_n1	AJ71C21 ready signal		Turns on when the AJ71C21 has become ready after power is switched on. Turns off in the offline mode with I/F mode selector switch.	○	○
X_n2	No protocol	RS-232C send end	Turns on when data has been sent from the AJ71C21 to the RS-232C equipment. Turns off when the request to send signal, $Y_{n+1}2$, turns off.	×	○
X_n3	No protocol	RS-232C receive data read request	Turns on when data from the RS-232C equipment has been received by the AJ71C21. Turns off when the receive data read end signal, $Y_{n+1}3$, is turned off.		
X_n4	No protocol	RS-232C receive data clear end	Turns on when the receive data from the RS-232C equipment has been cleared. Turns off when the receive data clear request signal, $Y_{n+1}4$, turns off.		
X_n5	RS-232C send buffer full		Turns on when the RS-232C transmission buffer is not vacant. Turns off when the transmission buffer is vacant.	×	○
X_n6	RS-232C receive buffer full		Turns on when the RS-232C receive buffer is full. Subsequent data from the receive buffer is discarded. Turns off when the receive buffer is not full.		
X_n7	No protocol	RS-422 send end	Turns on when data has been sent from the AJ71C21 to the RS-422 interface. Turns off when the request-to-send signal, $Y_{n+1}7$, turns off.	×	○
X_n8	No protocol	RS-422 receive data read request	Turns on when the data from the AJ71C21 has been received. Turns off when the received data read end signal, $Y_{n+1}8$, turns on.		
X_n9	No protocol	RS-422 receive data clear end	Turns on when the received data from the RS-422 equipment has been cleared. Turns off when the receive data clear request signal, $Y_{n+1}9$, signal turns off.		
X_nA	RS-422 send buffer full		Turns on when the RS-422 transmission buffer is not vacant. Turns off when the transmission buffer is vacant.	×	○
X_nB	RS-422 receive buffer full		Turns on when the RS-422 is full and subsequent data from the receive buffer is discarded. Turns off when the receive buffer is not full.		
X_nC	RAM write end		Turns on when data has been written in RAM. Turns off when the RAM write request signal, $Y_{n+1}C$, is turned off.	×	○
X_nD	RAM read end		Turns on when data has been read from RAM. Turns off when the RAM read request signal, $Y_{n+1}D$, turns off.		
X_nE	RAM error		Turns on when an error occurs while data is being written to and read from the RAM. Turns off when "0" is written at 5FCH in the buffer memory.		
X_nF	Battery error		Turns on when an AJ71C21 battery error occurs. Turns off when battery voltage is normal.	○	○

The signals marked with "○" can be used by users. On the other hand, signals marked with "×" cannot be used by users as they are used by the system.

Table 3.6 List of Input Signals

POINT

Y(Y_n0 to Y_nF) corresponding to X_n0 to X_nF may be used as internal relays.

(2) Output signal (PC CPU→AJ71C21)
Output signals number 16: $Y_{(n+1)}0$ to $Y_{(n+1)}F$.

Output Signal	Signal Designation		Description	BASIC Program Mode	Sequence Program Mode
$Y_{n+1}0$	--		Not used	×	×
$Y_{n+1}1$					
$Y_{n+1}2$	No protocol	RS-232C send request	When turned on by the sequence program, the data stored in the AJ71C21 buffer memory is sent to the RS-232C.	×	○
$Y_{n+1}3$		RS-232C receive data read end	Turns on when the receive data arriving from the RS-232C and stored in the AJ71C21 has been read.		
$Y_{n+1}4$		RS-232C receive data clear request	When turned on by the sequence program, clears the receive data from the RS-232C.		
$Y_{n+1}5$	--		Not used	×	×
$Y_{n+1}6$					
$Y_{n+1}7$	No protocol	RS-422 send request	When turned on by the sequence program, the data stored in the AJ71C21 buffer memory is sent to the RS-422.	×	○
$Y_{n+1}8$		RS-422 receive data read end	Turns on when the data arriving from the RS-422 and stored in the buffer memory has been read by the PC CPU.		
$Y_{n+1}9$		RS-422 receive data clear request	When turned on by the sequence program, the receive data from the RS-422 is cleared.		
$Y_{n+1}A$	--		Not used	×	×
$Y_{n+1}B$					
$Y_{n+1}C$	RAM write request		When turned on by the sequence program, the data stored in the buffer memory is written to the AJ71C21 RAM memory.	×	○
$Y_{n+1}D$	RAM read request		When turned on by the sequence program, the data stored in the AJ71C21 RAM memory is read into the buffer memory.		
$Y_{n+1}E$	--		Not used	×	×
$Y_{n+1}F$					

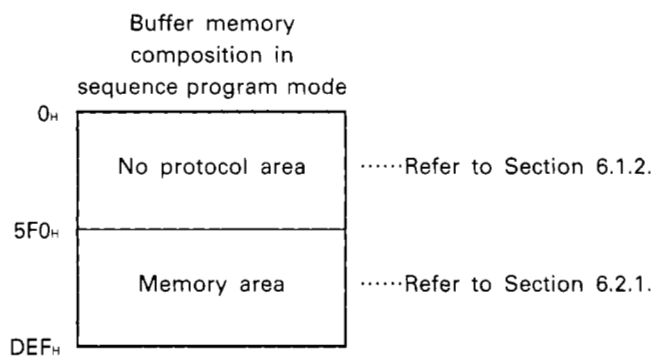
Table 3.7 List of Output Signals

IMPORTANT

The signals marked with "×" cannot be used by users as they are used by the system. If an attempt is made to use these signals in the sequence program (ON/OFF), the performance of the AJ71C21 cannot be guaranteed.

3.6 Buffer Memory

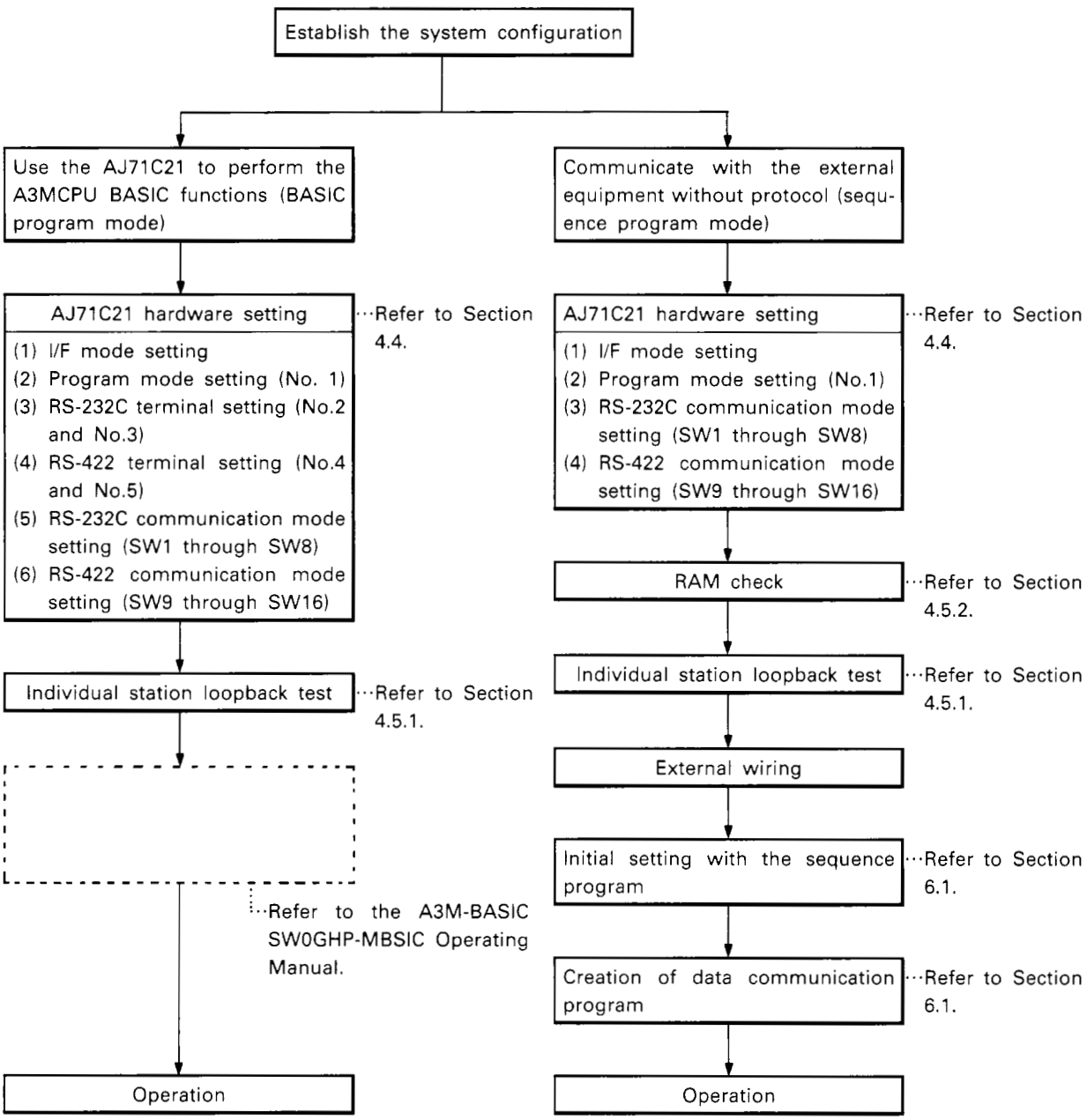
The AJ71C21 has a buffer memory (not battery backed) for communication of data with the PC CPU. The assignment of this buffer memory is described below.
The buffer memory assignment is as follows for the BASIC program mode and sequence program mode. The user cannot use the memory in the BASIC program mode, only in the sequence program mode.



4. SETTINGS AND PROCEDURES REQUIRED FOR OPERATION

4.1 Settings and Procedures Required for Operation

This section describes the settings and procedures required for starting up the system employing the AJ71C21 are described below.



IB (NA) 66198-A

4.2 Handling Precautions

This section describes the precautions to be taken when handling the AJ71C21.

(1) Use care not to let the AJ71C21 plastic casing and its terminal block fall. Do not subject them to undue impact.

(2) Do not attempt to remove the printed circuit board from the casing or a malfunction will result.

(3) Do not allow foreign matter, such as wire offcuts, to enter the module. If any are present, remove them from inside the module.

(4) Tighten the module mounting screw as indicated below (not required in normal use).

Screw	Tightening torque range kg·cm (lb·inch)
Module mounting screw (usually unnecessary) (M4)	8 (6.93) to 12 (10.4)

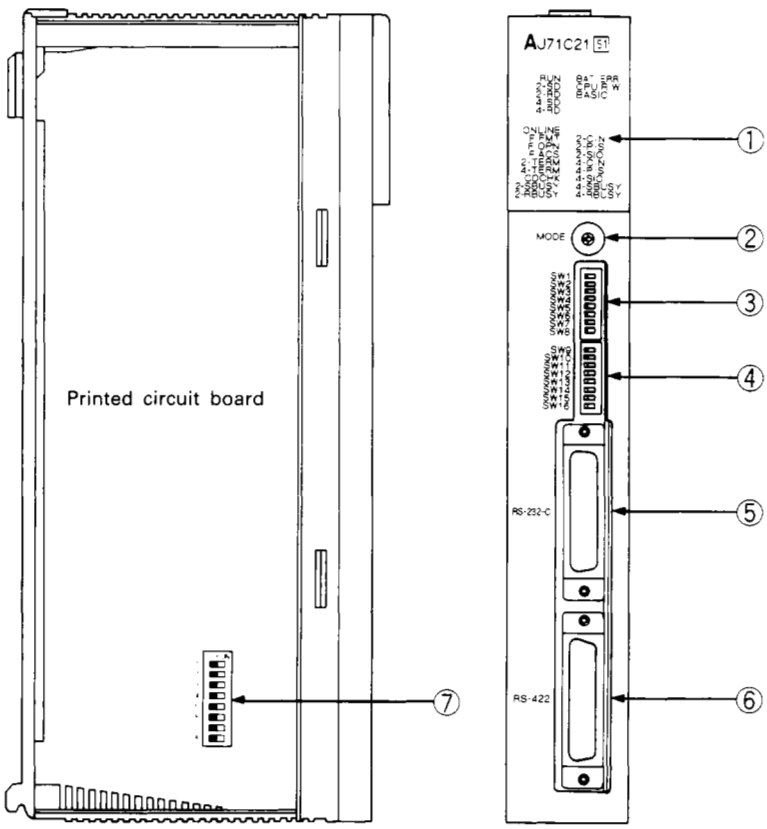
(5) When loading the module on the base, hook it to the base securely. To remove the module, completely unhook it before pulling it forward.

IB (NA) 66198-A

4.3 Nomenclature

The names of the AJ71C21 components and details of the LED display are given below.

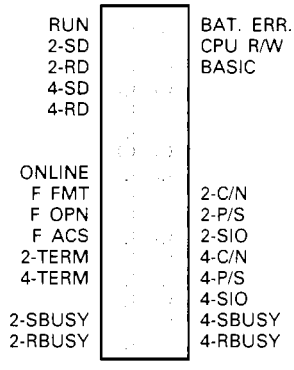
4.3.1 Nomenclature



No.	Component Name	Description	Refer to
①	Display LED	Used to display the operation status, conditions during link communication, error definitions, memory status, and other data.	Refer to Section 4.3.2
②	I/F mode setting switch	Used to select a desired I/F mode Set to "0" prior to shipment.	Refer to Section 4.4.1
③	RS-232C communication mode setting switch	Used to set the RS-232C communication specifications.	Refer to Section 4.4.3
④	RS-422 communication setting switch	Used to set the RS-422 communication specifications.	Refer to Section 4.4.4
⑤	RS-232C connector	For connection with external equipment.	Refer to Section 4.6.2
⑥	RS-422 connector	For connection with external equipment.	Refer to Section 4.6.3
⑦	I/F terminal setting switch	Used to set the program mode and RS-232C/RS-422 terminal.	Refer to Section 4.4.2

4.3.2 LED display

This section describes the LED designations and the meaning of LED display.



LED	Meaning of LED Display	LED ON	LED OFF	Initial State of LED	Mode in Use	
					BASIC	Sequence
RUN	Normal run display	Normal	Error	ON		
2-SD	RS-232C send status	Flickers during data sending.		OFF		
2-RD	RS-232C receive status	Flickers during data receiving.		OFF		
4-SD	RS-422 send status	Flickers during data sending.		OFF		
4-RD	RS-422 receive status	Flickers during data receiving.		OFF		
ON LINE	Online/offline status	Online	Offline	OFF		
F FMT	Memory format status	Lights when formatting is complete.		OFF		×
F OPN	Memory open status	File open	File close	OFF		×
F ACS	File access status	During file access	File not accessed	OFF		×
2-TERM	RS-232C connector	VT220/printer connected	GPP connected	OFF		×
4-TERM	RS-422 connector	VT220/printer connected	GPP connected	OFF		×
2-SBUSY	RS-232C send buffer status	Buffer is not vacant.	Buffer is vacant.	OFF		
*2-RBUSY	RS-232C receive buffer status	Buffer is full.	Buffer is not full.	OFF		
BAT.ERR.	Battery status	Error	Normal	OFF		
CPU R/W	Communication with PC	Flickers during communication with PC (remains lit when there is no communication)		ON		
BASIC	Program mode setting	BASIC program mode	Sequence program mode	OFF		
*2-C/N	Results of communication between RS-232C and PC CPU	Access error	Normal	OFF		
*2-P/S	RS-232C parity status	Parity error	Normal	OFF		
*2-SIO	RS-232C SIO status	Overrun, framing error	Normal	OFF		
*4-C/N	Results of communication between RS-422 and PC CPU	Access error	Normal	OFF		
*4-P/S	RS-422 parity status	Parity error	Normal	OFF		
*4-SIO	RS-422 SIO status	Overrun, framing error	Normal	OFF		
4-SBUSY	RS-422 send buffer status	Buffer is not vacant.	Buffer is vacant.	OFF		
*4-RBUSY	RS-422 receive buffer status	Buffer is full.	Buffer is not full.	OFF		

The LEDs marked with * remain lit after normal condition have been restored.

Table 4.1 LED Display

4.4 Switch Settings

This section describes how to set the communication specifications and relevant switches.
When the setting has been changed, change the PC CPU power switch position from OFF to ON or reset the PC CPU. For examples of switch settings, refer to Sections 2.3 and 2.4.

4.4.1. I/F mode setting

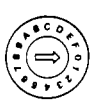
Mode Setting Switch	Mode Setting Switch Number	Setting			Remarks
		BASIC program mode		Sequence program mode	
	0	Online	RS-422 console RS-232C general-purpose port	Online	Set to mode "0" prior to shipment.
	1	Online	RS-422 general-purpose port RS-232C console	Not used	
	2	Online	RS-422 general-purpose port RS-232C general-purpose port	Not used	
	3	Offline File access with GPP		Memory backup by offline GPP	1. GPP allows connection with the RS-422 only. Upon connection with the GPP, the communication specifications are switched to automatic setting mode. 2. The RS-232C can be used as a general-purpose port (provided that the mode has been changed from online to offline).
	4 to 7	Not used			
	8	For line test			RS-422/RS-232C communication check
	9	For RAM check			Used for the AJ71C21-S1 only
	A	For delivery inspection			
	B to F	Not used			

Table 4.2 I/F Mode Setting

(1) It is not necessary to change the PC CPU power switch position from OFF to ON or reset the CPU for mode change purposes under either of the following conditions.
Online mode (0,1,2)→Offline mode (3)
Online mode (0,1,2)→Offline mode (3)→Online mode (0,1,2)
(The mode becomes online when the original switch number is selected. The mode remains offline when the Switch number other than the original one is selected.)

(2) When the system has been started up in the offline mode (3), the mode connot be changed to online, first change the mode swich position to online (0,1, or 2) and then reset the CPU.

B (NAI 66198-A

4.4.2 Program mode and RS-232C/RS-422 terminal settings

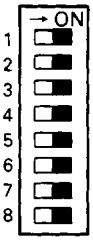
<table>
<tr><th rowspan="2">Appearance of Setting Switch</th><th rowspan="2">Setting Switch</th><th rowspan="2">Setting</th><th colspan="2">Setting Switch Position</th><th rowspan="2">Remarks</th><th colspan="2">Necessity of Switch Setting</th></tr>
<tr><th>OFF</th><th>ON</th><th>BASIC program mode</th><th>Sequence program mode</th></tr>
<tr><td rowspan="8">  </td><td>No. 1</td><td>Program mode setting</td><td>Sequence program mode</td><td>BASIC program mode</td><td></td><td>○</td><td>●</td></tr>
<tr><td>No. 2</td><td rowspan="2">RS-232C terminal setting</td><td colspan="3" rowspan="2"><table><tr><th>Type connected</th><th>VT-220</th><th>Not used</th><th>Not used</th></tr><tr><td></td><td>OFF</td><td>OFF</td><td>ON</td></tr><tr><td></td><td>OFF</td><td>ON</td><td>ON</td></tr></table></td><td rowspan="2">Valid in the BASIC program mode only</td><td rowspan="2">○</td><td rowspan="2"></td></tr>
<tr><td>No. 3</td></tr>
<tr><td>No. 4</td><td rowspan="2">RS-422 terminal setting</td><td colspan="3" rowspan="2"><table><tr><th>Type connected</th><th>VT-220</th><th>Not used</th><th>GPP</th></tr><tr><td></td><td>OFF</td><td>OFF</td><td>ON</td></tr><tr><td></td><td>OFF</td><td>ON</td><td>ON</td></tr></table></td><td rowspan="2"></td><td rowspan="2">○</td><td rowspan="2"></td></tr>
<tr><td>No. 5</td></tr>
<tr><td>No. 6</td><td rowspan="3">Not used</td><td colspan="3" rowspan="3">—</td><td rowspan="3">—</td><td rowspan="3">—</td><td rowspan="3">—</td></tr>
<tr><td>No. 7</td></tr>
<tr><td>No. 8</td></tr>
</table>

Table 4.3 Program Mode and Terminal Settings

(1) When the GPP is connected to the RS-422 port, it is not necessary to set the communication specifications since the GPP specifications are automatically set.

(2) Have the RS-232C/RS-422 converter on hand when connecting the VT-220 to the RS-422 port.

IB (NA) 66198-A

4.4.3 RS-232C/RS-422 communication mode setting

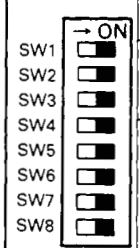
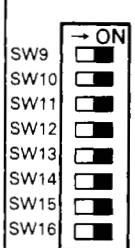
<table>
<tr><th rowspan="2">Appearance of Setting Switch</th><th rowspan="2">Setting Switch</th><th rowspan="2">Setting</th><th colspan="2">Setting Switch Position</th><th rowspan="2">Remarks</th><th colspan="2">Necessity of Switch Setting</th></tr>
<tr><th>OFF</th><th>ON</th><th>BASIC program mode</th><th>Sequence program mode</th></tr>
<tr><td rowspan="8">  </td><td>SW1</td><td>RS-232C data bit setting</td><td>7 bits</td><td>8 bits</td><td></td><td rowspan="8">○</td><td rowspan="8">○</td></tr>
<tr><td>SW2</td><td rowspan="3">RS-232C transmission speed setting</td><td colspan="2" rowspan="3"><table><tr><th>Baud rate</th><th>Not used</th><th>600</th><th>1200</th><th>2400</th><th>4800</th><th>9600</th><th>19200</th><th>Not used</th></tr><tr><td></td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td></tr><tr><td></td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td></tr><tr><td></td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr></table></td><td rowspan="3"></td></tr>
<tr><td>SW3</td></tr>
<tr><td>SW4</td></tr>
<tr><td>SW5</td><td>RS-232C parity check</td><td>No</td><td>Yes</td><td></td></tr>
<tr><td>SW6</td><td>RS-232C parity setting</td><td>Odd</td><td>Even</td><td>Valid only when parity check on is selected</td></tr>
<tr><td>SW7</td><td>RS-232C stop bit setting</td><td>1 bit</td><td>2 bits</td><td></td></tr>
<tr><td>SW8</td><td>Communication control setting</td><td>XON/XOFF</td><td>DTR terminal</td><td></td></tr>
<tr><td rowspan="8">  </td><td>SW9</td><td>RS-422 data bit setting</td><td>7 bits</td><td>8 bits</td><td></td><td rowspan="8">○</td><td rowspan="8">○</td></tr>
<tr><td>SW10</td><td rowspan="3">RS-422 transmission speed setting</td><td colspan="2" rowspan="3"><table><tr><th>Baud rate</th><th>Not used</th><th>600</th><th>1200</th><th>2400</th><th>4800</th><th>9600</th><th>19200</th><th>Not used</th></tr><tr><td></td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td></tr><tr><td></td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td></tr><tr><td></td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr></table></td><td rowspan="3"></td></tr>
<tr><td>SW11</td></tr>
<tr><td>SW12</td></tr>
<tr><td>SW13</td><td>RS-422 parity check</td><td>No</td><td>Yes</td><td></td></tr>
<tr><td>SW14</td><td>RS-422 parity setting</td><td>Odd</td><td>Even</td><td>Valid only when parity check is selected</td></tr>
<tr><td>SW15</td><td>RS-422 stop bit setting</td><td>1 bit</td><td>2 bits</td><td></td></tr>
<tr><td>SW16</td><td>Communication control setting</td><td>XON/XOFF</td><td>DTR terminal</td><td></td></tr>
</table>

Table 4.4 RS-232C/RS-422 Communication Mode Setting

POINT

During the XON/XOFF control, do not include the XON (11H)/ XOFF (13H) code in the data since it is considered a control code and processed as such.
When this code is in need as data, use the DTR control.

4.5 Test Mode

This section describes the AJ71C21 individual station communication check and RAM check.

4.5.1 Individual station loopback test

The term "individual station loopback test" is the function that tests whether the single AJ71C21 functions normally without any external equipment. This function can be performed when the I/F mode setting switch is set to "8".
The procedures for the single station loopback test are described below.

(1) Cable connections
Connect the cable to the RS-232C/RS-422 connector as indicated below.

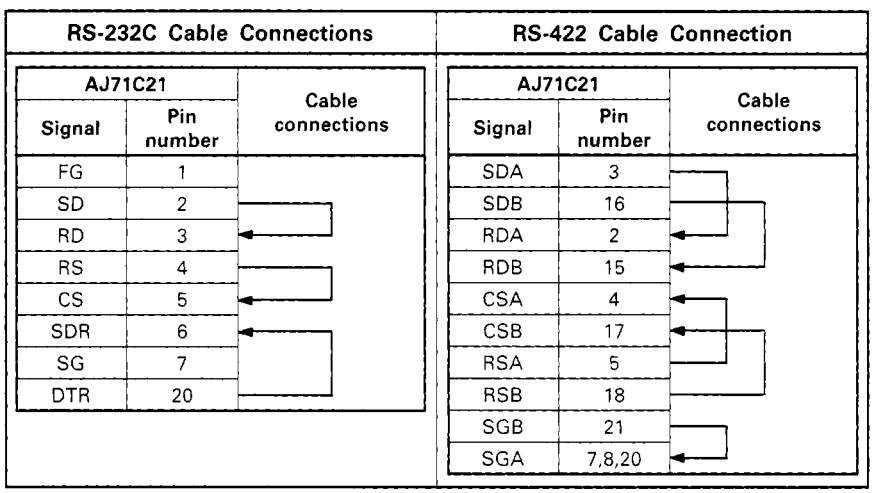


Fig. 4.1 RS-232C/RS-422 Cable Connections

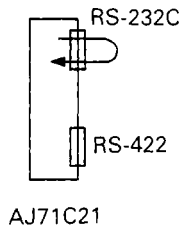
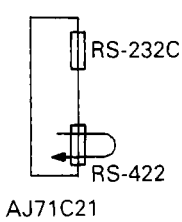
(2) I/F mode setting switch setting
Set the mode setting switch to "8" for the line test (for details, refer to Section 4.4.1).

(3) Single station loopback test
1) Setting the PC CPU power switch to the ON position or resetting the CPU turns on the AJ71C21 ready signal, starting an automatic check.
2) Order of Check
In check proceeds from the RS-232C to the RS-422. This procedure is repeated. (The AJ71C21 automatically executes this check.)
3) Check the LED display on the AJ71C21 front panel.
Normal: The test is finished.
Error: Conduct the test again after removing the cause of the error.
4) Step Required on Completion of the Test
Switch off the power, disconnect the cable, and change the mode setting switch position.

REMARKS

The individual station loopback test can be made when two or more modules are mounted.

The check items for individual station loopback test and the LED display indicating normal or error status are as shown in Table 4.5.

Items	Check	Normal Operation LED		Error Indicator LED		Remarks
RS-232C communication check	The data sent from the AJ71C21 RS-232C connector is received by the RS-232C connector. If the data matches, it is then changed by the AJ71C21 and sent. This procedure is repeated. If the data does not match, an error is indicated. Error indication also appears when the cable is disconnected.	2-SIO	OFF	2-SIO	ON	
		2-SD	Flickers			
		2-RD				
RS-422 communication check	The data sent from the AJ71C21 RS-422 connector is received by the RS-422 connector. If the data matches, it is changed by the AJ71C21 and sent. This procedure is repeated. If the data does not match, an error is indicated. Error indication also appears when the cable is disconnected.	4-SIO	OFF	4-SIO	ON	
		4-SD	Flickers			
		4-RD				

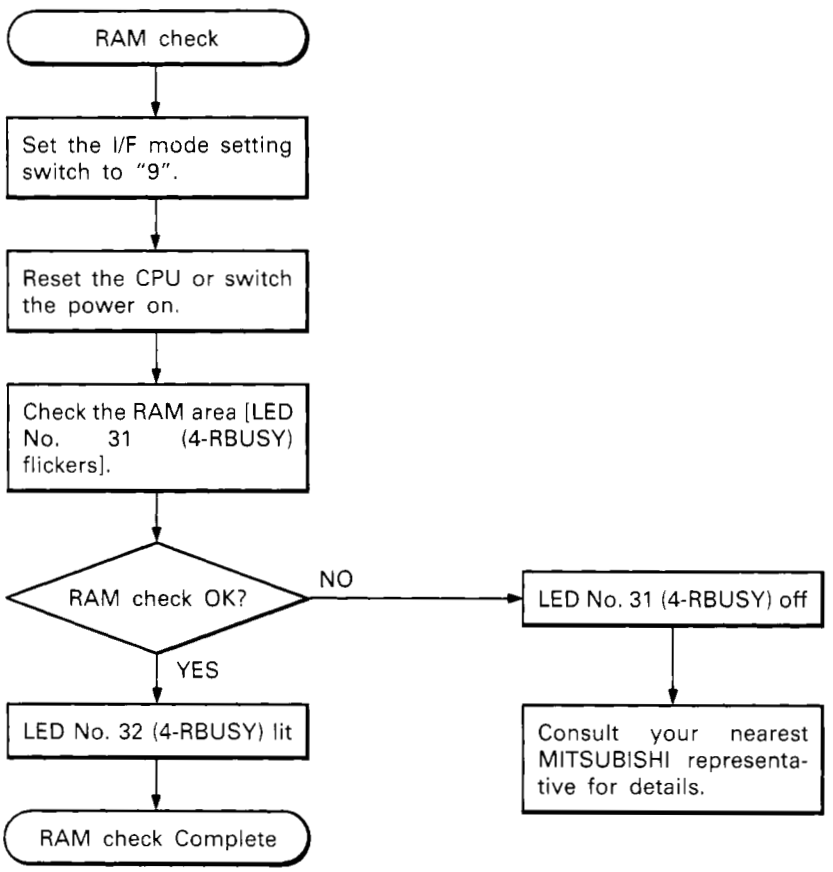
*The test is not interrupted when an error is indicated during any check.

Table 4.5 Individual Station Loopback Test

4.5.2 RAM check

The RAM check is the function that checks for faults in the AJ71C21-S1 RAM. This function can be performed when the I/F mode setting switch is set to "9".

Data is written in all areas ranging from the head to the final RAM area in 1-byte steps and read. The RAM is checked by verifying the data. (This procedure takes approximately 3 minutes.)



POINT

(1) Prior to using the AJ71C21-S1 for the first time, check and initialize the RAM.

(2) Checking the RAM will clear all the data stored in it.

4.6 Wiring Connections

4.6.1 Wiring precautions

To obtain optimum performance and make the AJ71C21 a highly reliable system, noise-resistant external wiring is indispensable. Take the following precautions when connecting external wiring for the AJ71C21.

(1) Keep data carrying cables at least 100mm away from main circuit wiring, high voltage cables, and load carrying wires leading from equipment other than the PC. Do not bundle the data carrying cable with other cables.
If the above precautions are not taken, the AJ71C21 will be subject to adverse effects induced by noise or surge induction.

(2) Ground shielded wires or cable shields at one point only.

4.6.2 RS-232C connector connections

Typical examples of RS-232C connections are given below.

(1) DTR terminal is set according to the communication control setting.

AJ71C21		Cable Connection and Signal Direction	Computer		Description
Signal	Pin No.		Pin No.	Signal	
FG	1		1	FG	Frame ground
SD(TXD)	2		2	SD(TXD)	Send data
RD(RXD)	3		3	RD(RXD)	Receive data
RS	4		4	RS	Request to send
CS(CTS)	5		5	CS(CTS)	Clear to send
DSR(DR)	6		6	DSR(DR)	Data set ready
SG	7		7	SG	Signal ground
DTR(ER)	20		20	DTR(ER)	Data terminal ready

Fig. 4.2 RS-232C Connections (DTR Terminal Setting)

(2) XON/XOFF is set according to the communication control setting.

AJ71C21		Cable Connection and Signal Direction	Computer	
Signal	Pin No.		Pin No.	Signal
FG	1		1	FG
SD(TXD)	2		2	SD(TXD)
RD(RXD)	3		3	RD(RXD)
RS	4		4	RS
CS(CTS)	5		5	CS(CTS)
DSR(DR)	6		6	DSR(DR)
SG	7		7	SG
DTR(ER)	20		20	DTR(ER)

Fig. 4.3 RS-232C Connections (XON/XOFF Setting)

4.6.3 RS-422 connections

Typical examples of the RS-422 connections are given below.

AJ71C21			Cable Connection and Signal Direction	Computer		Description
Signal (reversed)	Signal (normal)	Pin No.		Pin No.	Signal	
$\overline{SDA}$	SDA	3		2	RDA	Receive data
$\overline{SDB}$	SDB	16		15	RDB	Receive data
$\overline{RDA}$	RDA	2		3	SDA	Send data
$\overline{RDB}$	RDB	15		16	SDB	Send data
$\overline{CSA}$	CSA	4		5	RSA	Request to send
$\overline{CSB}$	CSB	17		18	RSB	Request to send
$\overline{RSA}$	RSA	5		4	CSA	Clear to send
$\overline{RSB}$	RSB	18		17	CSB	Clear to send
SGB	SGB	21		21		
SGA	SGA	7,8,20		7,8,20	SG	Signal ground
FG	FG	1		1	FG	Frame ground

*Be sure to connect the wire leading from pin No. 21 to the signal ground of the connected equipment.

Fig. 4.4 RS-422 Connections

4.7 Inspection and Maintenance

4.7.1 Battery replacement (for the AJ71C21-S1 only)

If a battery voltage is too low, the LED "BAT.ERR" on the AJ71C21 front panel will light.
A power failure, indicated by LED "BAT.ERR" does not present problems for short periods, but, if allowed to continue for prolonged time, data stored in the built-in RAM will be destroyed. To avoid such a situation, it is recommended that the low-voltage battery be replaced as soon as possible to prevent malfunctions.

	Guaranteed value (minimum)
Battery guarantee period	5 years
Backup by battery	29 days
Backup by capacitor	1.3 min

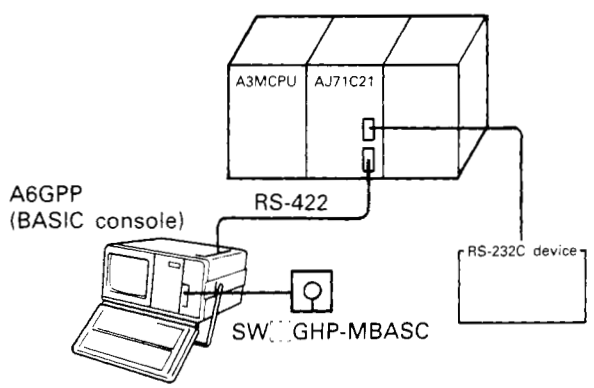
5. BASIC PROGRAM MODE

This section describes the functions performed in the BASIC program mode.

5.1 The BASIC Console

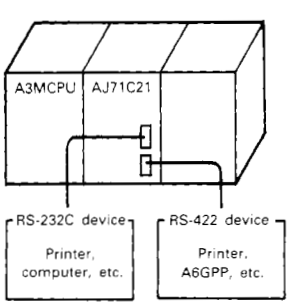
The A3MCPU alone is capable of processing sequence and BASIC programs in parallel.
The AJ71C21 serves as an I/F when the GPP or VT220 is used as a console for BASIC in compliance with the BASIC functions performed by the A3MCPU.
The BASIC console allows the development of the BASIC program, data input in response to the input request, and data output from the A3MCPU with the BASIC instruction.
For details on setting the AJ71C21 hardware, refer to Sections 4.4 and 2.3.

(1) A6GPP used as BASIC console



5.2 General-Purpose Port

The AJ71C21 is provided with one RS-232C port and one RS-422 port and can be connected with the RS-232C and RS-422 equipment as a general-purpose port.
For details on the setting the AJ71C21, refer to Section 4.4.



IB (NA) 66198-A

5.3 File I/O (for the AJ71C21-S1 only)

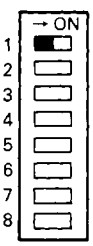
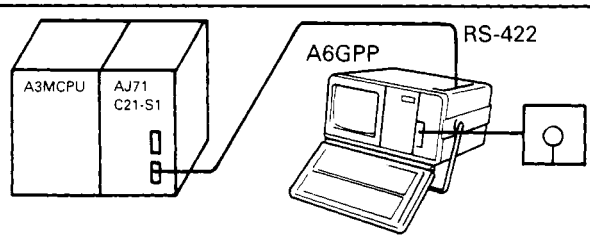
The AJ71C21-S1 built-in RAM can be used as a file memory which allows file operation through the GPP and file access with the BASIC instruction from the A3MCPU.

(1) File operation through GPP

(a) Connecting the AJ71C21-S1 and GPP

Set the I/F mode setting switch on the AJ71C21-S1 front panel to the "3" position and set the inner program mode setting switch No. 1 to the ON position (BASIC program mode).

Connect the AJ71C21-S1/RS-422 connector and the GPP using the AC30R4 cable.

Switch Setting		System Configuration
Mode setting	Program mode setting	
		 Start up the system with SW□GHP-MBASC.

(b) File operation

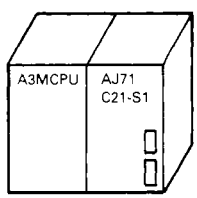
The following file operations can be performed from the GPP to the AJ71C21-S1. For details, refer to the Type SW0GHP-MBASC A3M-BASIC Operating Manual.

- Directory display
- File delete
- File copy (GPP ⟷ RAM files)
- File verify
- Format

(2) File operation by the A3MCPU (BASIC)

(a) Switch setting

Set the I/F mode setting switch on the AJ71C21-S1 front panel to the "0","1", or "2" position and set the inner program mode setting switch No. 1 to the ON position (BASIC program mode).

Switch Setting		System Configuration
Mode setting	Program mode setting	
The mode may be set to either 0, 1, or 2.		

(b) File access with the BASIC instruction

Files can be accessed from the A3MCPU with the BASIC instruction. For details, refer to the A3M-BASIC Programming Manual.

(3) Files cannot be accessed from the A3MCPU/GPP to the AJ71C21 that does not contain RAM. If an attempt is made to gain such access, an error is indicated on the A3MCPU/GPP.

(4) When the I/F mode setting switch is set at "3", X_n1 (AJ71C21 ready signal) is turned off.

6. SEQUENCE PROGRAM MODE

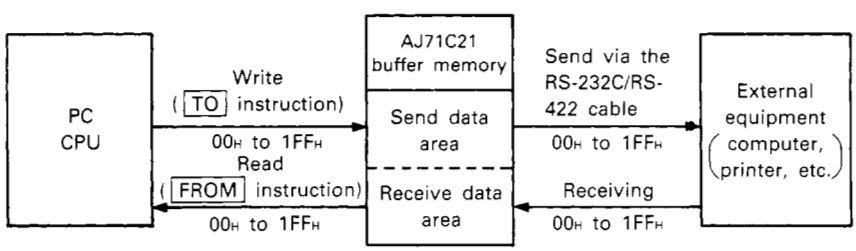
The functions performed in the sequence program mode are described below.

6.1 Communication with External Equipment in the No Protocol Mode

6.1.1 Basics in no protocol mode

This section describes the basics required when the external equipment (computer, printer, etc.) is to be linked with the PC CPU in the no protocol mode.

(1) What is "no protocol"?
The term "no protocol" means the procedure in which the data written in the no protocol send data area in the AJ71C21 buffer memory from the PC CPU with the TO instruction is output in the identical code to the external equipment or the data arriving from the external equipment is read by the CPU from the no protocol receive data area in the AJ71C21 buffer memory with the FROM instruction.



POINT

Since the AJ71C21 does not convert data into ASCII, the PC CPU needs to be able to handle data in ASCII code beforehand when such coded data is needed.

(2) Word/byte specification for no protocol communication data
Transmission data can be specified in either word or byte units in the no protocol mode. Send data, as the default value, is preset in word units. This setting, however, can be changed by writing "0" or "1" at 202H/212H in the buffer memory specific-use area.
(For details on the setting program, refer to Section 6.1.7.)

6.1.2 Buffer memory

The term "buffer memory" refers to the AJ71C21 memory area which is used to communicate data between the PC CPU and external equipment, such as a computer.
The AJ71C21 stores data sent from the external equipment via the OS area in the no protocol send buffer memory area.
The receive data is stored in the OS area until it is in the condition that permits its transfer to the no protocol send buffer memory (request-to-read X_n3 is turned off). The data up to the end code or equal in amount to the fixed-length data is transferred in either of the following conditions.

① The data overflows the buffer memory area when the no protocol send area is greater than the received data length.
② Before the PC CPU finishes reading the data received once, the external equipment sends the next data.

(1) Applications of buffer memory
The buffer memory has two areas: the area used by the user and the area used for predetermined purposes.

(a) Area for user's free use
The area for user's free use is classified into the following two subareas.
1) No protocol mode data send area
This area stores data sent from the external equipment in the no protocol mode.
2) No protocol mode data receive area
This area stores data sent to the external equipment from the PC CPU.

(b) Area for specific purposes
The use of this area is predetermined. In this area, the format for data communication is selected or the assignment of the memory area referred to in Section (a) above is changed.
The default value is written in the specific-purpose area when the power is switched on or when the PC CPU is reset.
The default value can be changed in accordance with the purpose of transmission, intended application, and specifications of the external equipment.

IB (NA) 66198-A

(2) Buffer memory assignment

The buffer memory is a 1-address 16-bit configuration. It is not backed up.

The designation and default value of each address in the buffer memory are listed in the table below.

Address	Designation of buffer memory address			Default value	
0H	For RS-232C	User's free area (256 words)	No protocol send data number storage area	0	
1H to 7FH			Buffer memory area for no protocol send		
80H			No protocol send data number storage area		
81H to FFH			Buffer memory area for no protocol receive		
100H	For RS-422	User's free area (256 words)	Default assignment	0	
101H to 17FH			Buffer memory area for no protocol send		
180H			No protocol send data number storage area		
181H to 1FFH			Buffer memory area for no protocol receive		
200H	For both RS-232C and RS-422	Error LED display area		0	·····Section 6.1.5
201H		Error LED off area		0	·····Section 6.1.6
202H	For RS-232C	No protocol word/byte specification area		0 (word)	·····Section 6.1.7
203H		No protocol send buffer memory head address specification area		0	···Section 6.1.8
204H		No protocol send buffer memory length specification area		80H	
205H		No protocol receive buffer memory head address specification area		80H	···Section 6.1.9
206H		No protocol receive buffer memory length specification area		80H	
207H		No protocol receive end data number specification area		127 (word)	·····Section 6.1.10
208H		No protocol receive end code specification area		0D0AH (CR, LF)	·····Section 6.1.11
209H to 211H		System area (not used)		———	
212H	For RS-422	No protocol word/byte specification area		0 (word)	·····Section 6.1.7
213H		No protocol send buffer memory head address specification area		100H	···Section 6.1.8
214H		No protocol send buffer memory length specification area		80H	
215H		No protocol receive buffer memory head address specification area		180H	···Section 6.1.9
216H		No protocol receive buffer memory length specification area		80H	
217H		No protocol receive end data number specification area		127 (word)	·····Section 6.1.10
218H		No protocol receive end code specification area		0D0AH (CR, LF)	·····Section 6.1.11
219H to 21FH		System area (not used)		———	
220H to 5EFH		User's free area		0	

Table 6.1 Buffer Memory List

IMPORTANT

Do not write data in the buffer memory at addresses 209H through 211H and 219H through since these addresses are for use by the system.
If data is written at such addresses, the AJ71C21 will not properly function.

6.1.3 Program creation precautions

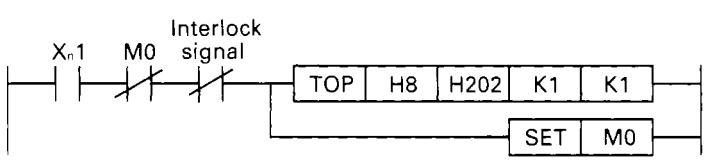
Take the following precautions when writing data in the buffer memory specific-use area with the sequence program.

(1) Data write in the specific-purpose area is valid only when the TO instruction of the sequence program is used.
No write can be made from the computer.

(2) The buffer memory is not backed up by the battery.
All data rewritten is changed back to default values when the power is switched on or when the CPU is reset.
It is necessary to write the set or changed data each time the power is switched on or the CPU is reset.

(3) Do not use buffer memory addresses 209_H through 211_H and 219_H through $21F_H$ which constitute the system area.
Do not write data at those addresses or the AJ71C21 will not properly function.

(4) Changing the set data of each data item is allowed only when the AJ71C21 ready signal (X_n1) rises as indicated below after the power is switched on or after the CPU is reset.
If an attempt is made to change the data during communication between the external equipment and the AJ71C21, the AJ71C21 will not function properly.
Example: Setting is "RS-232C byte specification."



6.1.4 Handshake I/O signals

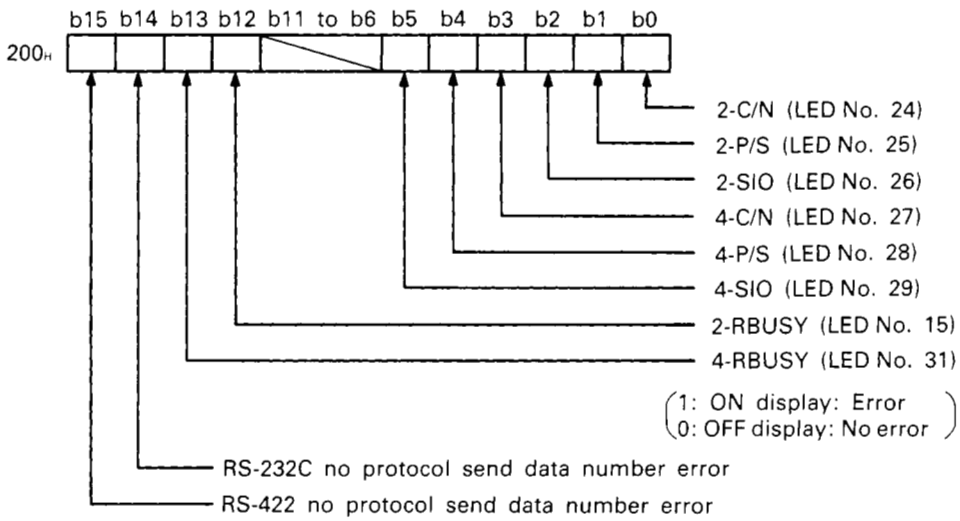
The handshake I/O signals include the signal which sends the data arriving from the PC CPU to the external equipment at the time of data communication in the no protocol mode or the signal by which the PC CPU is capable of reading the data arriving from the external equipment. Those signals are indispensable in the no protocol mode.
The handshake I/O signals are detailed below.

	Signal		Timing
PC CPU ↓ External equipment	$Y_{(n+1)}$ 2, 7	(send request)	Turned on with the program; Turned off with the program
	X_n 2, 7	(send end)	Turned on with the AJ71C21
External equipment ↓ PC CPU	X_n 3, 8	(receive data read request)	Turned on with the AJ71C21; Turned off with the program
	$Y_{(n+1)}$ 3, 8	(receive data read end)	Turned on with the program

IB (NA) 66198 A

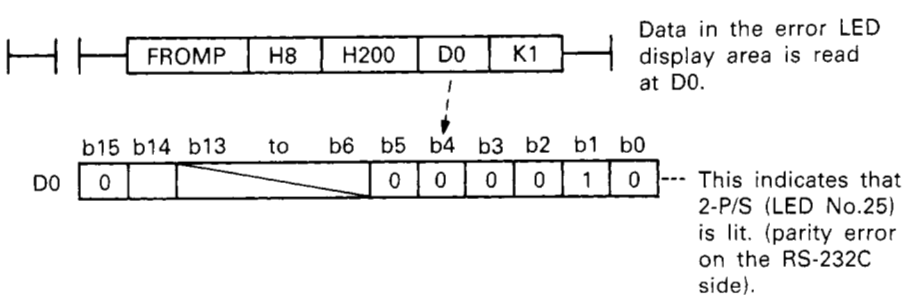
6.1.5 Error LED display status read

(1) Error LED display area
The error LED ON/OFF status is stored at address 200H in the buffer memory as follows.



(2) Example of error LED display area read program
The following is an example of the program with which the error LED ON/OFF status stored at buffer memory address 200H is read in response to the FROM instruction of the sequence program.

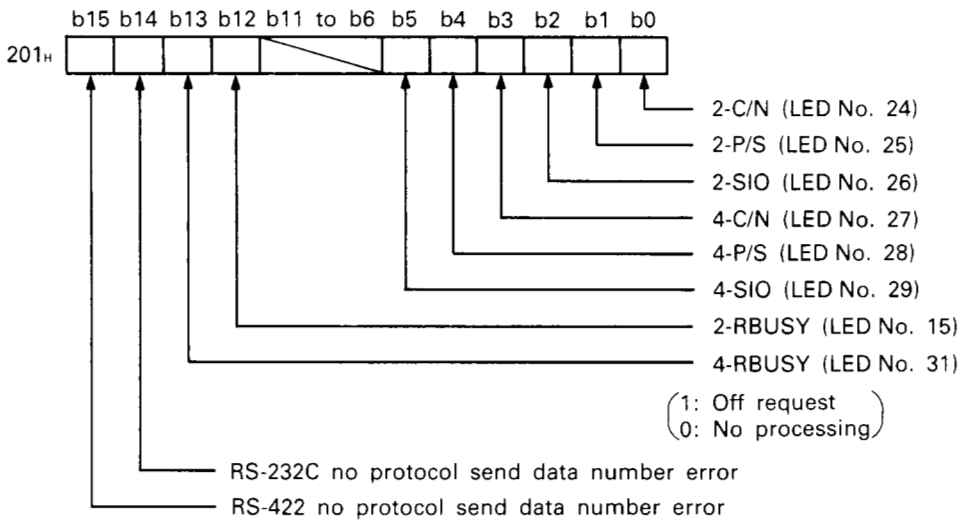
Example of the error LED display area read program (I/O addresses 80 through 9F in the AJ71C21)



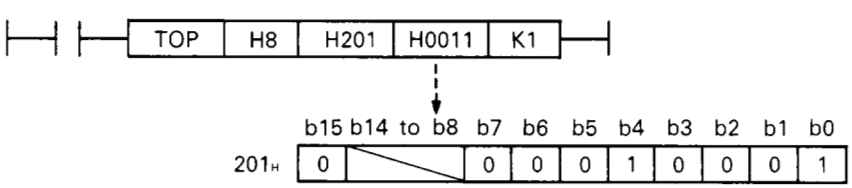
6.1.6 Error LED off

The error LED will remain lit even after normal status has been restored once it is lit.
A lit error LED can be turned off by writing "1" into the bit corresponding to the off request area at buffer memory address 201_H.

(1) Error LED off request area



(2) Example of error LED off request program
Example of sequence program (OFF request is made of 2-C/N (LED No.24) and 4-P/S (LED No.28))



POINT

(1) Off request is valid only when write is executed.
(2) Making an off request clears the data stored at error LED display area 200_H. However, the data stored at 201_H will remain intact.
(3) The error LED lights again when the error definition still remains at the time of off request.

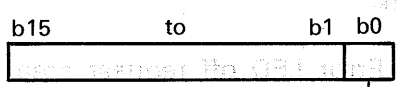
IB (NA) 66198 A

6.1.7 Word/byte specification

This section describes the method for and an example of specifying the setting of communication data in either word or byte units.

Specification Method

Buffer memory address 202H/212H



(Default 0: Word units)

0: Word units
1: Byte units

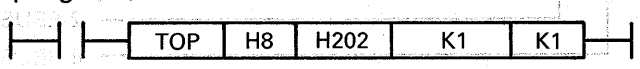
POINT

15 bits ranging from b1 to b15 at address 202H/212H may be 0 or 1 (the AJ71C21 will ignore this difference).

Specification Example

To handle data in byte units (AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C)

(Sequence program)

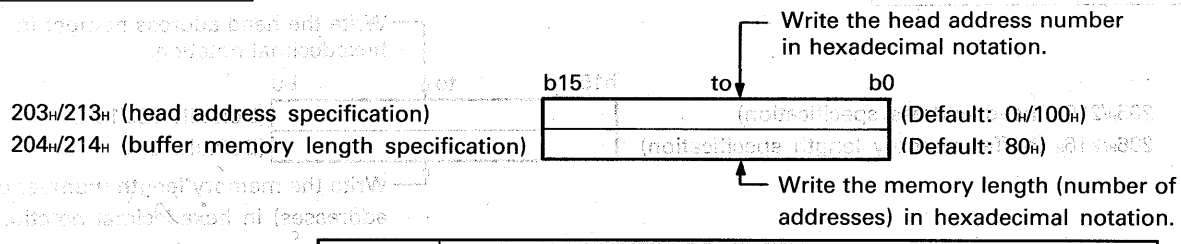


Write 1 : byte units at buffer memory address 202H.

6.1.8 Send buffer memory area setting

This section describes the method for and an example of specifying the AJ71C21 buffer memory area setting for storing the data to be sent from the PC CPU to the external equipment.

Specification Method



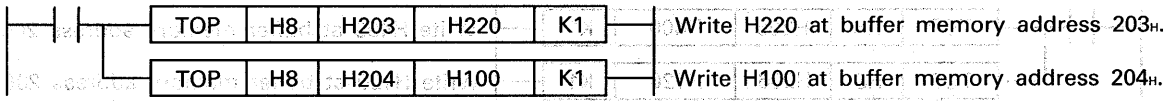
POINT

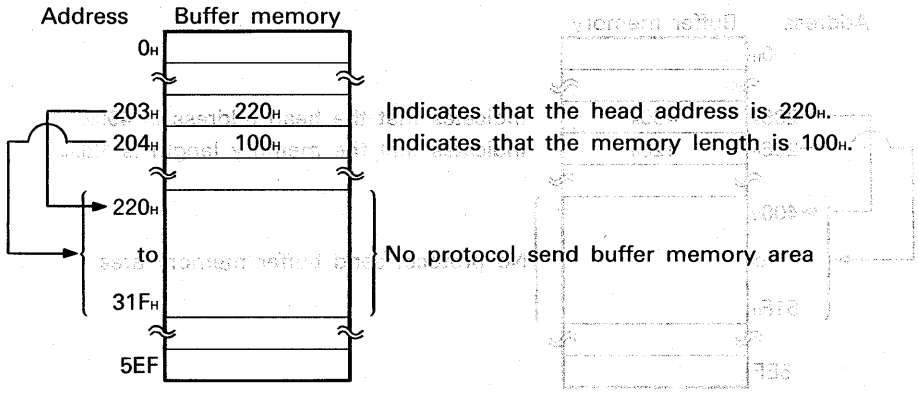
(1) Do not specify buffer memory addresses 200H through 21FH since these addresses constitute the specific-purpose area.
(2) Use care so that the specified range does not overlap the no protocol receive buffer memory area.
(3) When data outside the range (other than 00 through 5EF) is specified, the data in the AJ71C21 is processed as default values.

Specification Example

To specify 220H for head address and 100H for memory length (the AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C)

(Sequence program)

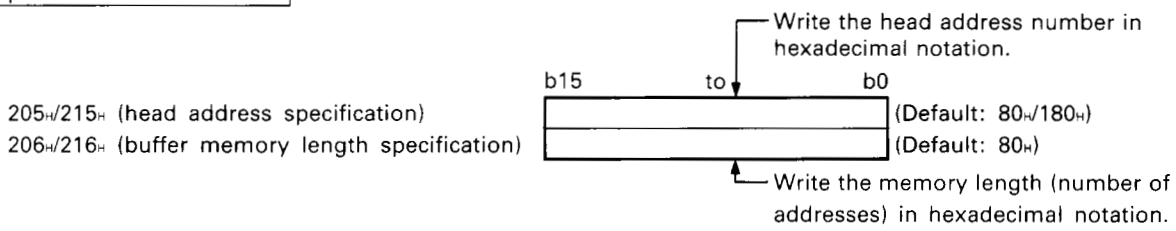




6.1.9 Receive buffer memory area setting

This section describes the method for and an example of specifying the AJ71C21 buffer memory area setting for storing the data to be sent from the external equipment to the PC CPU.

Specification Method



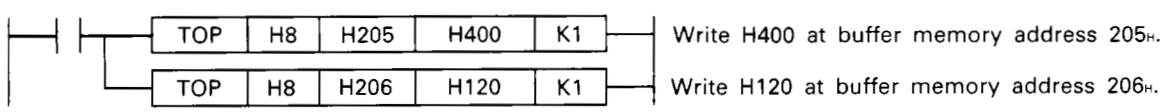
POINT

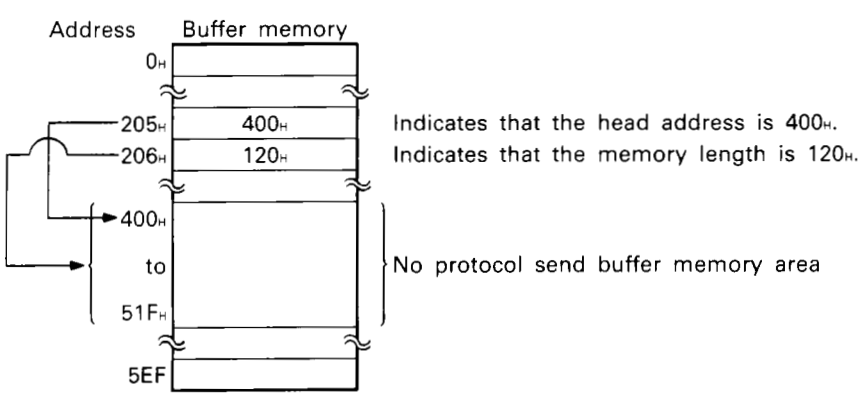
(1) Do not specify buffer memory addresses 200H through 21FH since these addresses constitute the specific-purpose area.
(2) Use care so that the specified range does not overlap the no protocol receive buffer memory area.
(3) When data outside the range (other than 00 through 5EF) is specified, the data in the AJ71C21 is processed as default values.

Specification Example

To specify 400H for head address and 120H for memory length (the AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C)

(Sequence program)

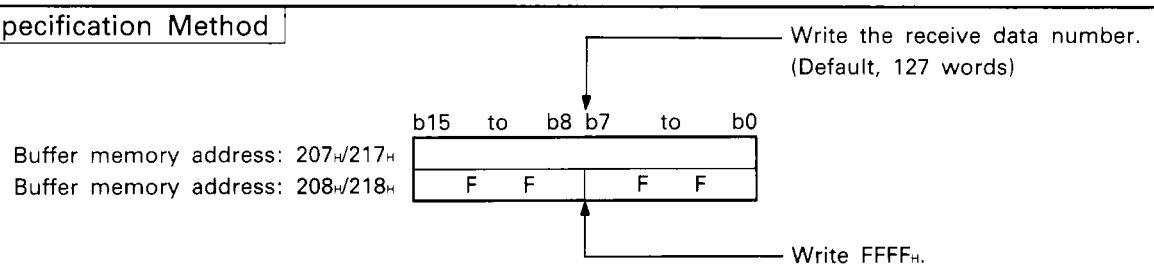




6.1.10 Receive end data number (fixed length) setting

This section describes the method for setting the receive based on fixed length and the receive data number and gives an example of the sequence program.

Specification Method



POINT

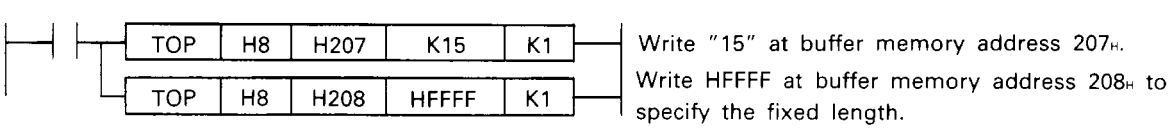
(1) Set the receive data number range as follows.
Receive data number ≦ no protocol buffer memory length−1 (in word units)
Receive data number ≦ (no protocol buffer memory length−1) ×2 (in byte units)
When the receive data number exceeds the no protocol receive buffer memory length, the value of the no protocol receive buffer memory length becomes the receive end data number.

(2) The choice between the word and the byte units depends on the specification described in Section 6.1.7.

Specification Example

To set the receive data number to 15 words for receiving based on the fixed length (AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C)

(Sequence program)



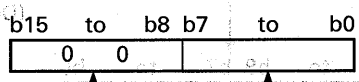
IB (NA) 66198-A

6.1.11 Receive end code setting

This section describes the specification method for setting and changing the end code and gives an example of the sequence program.

Specification Method

Buffer memory address: 208H/218H



(Default: 0D0AH (CR, LF))

Write any desired end code.

Be sure to write 00H into the upper 8 bits.

POINT

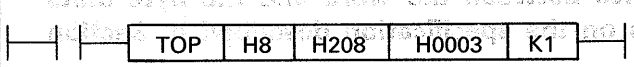
(1) The end code can be changed as desired over the range of 00H to 1FFH.

(2) With the preset receive end data number setting, the receive ends when either the end code or set data number is reached, whichever comes first.

Specification Example

To change the end code to ETX(03H) (AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C)

(Sequence program)



Write ETX ASCII code (03H) at buffer memory address 208H.

6.1.12 Send in no protocol mode (AJ71C21→computer)

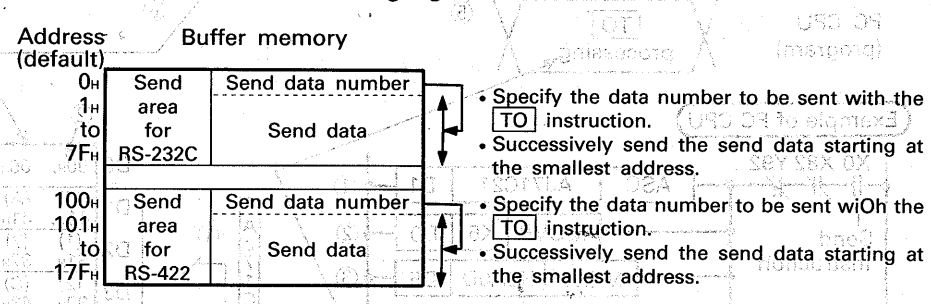
The "send" occurs when, in response to the send request signal ($Y_{(n+1)}2/Y_{(n+1)}7$) from the PC CPU, the AJ71C21 outputs data to the external equipment that is written in accordance with the TO instruction from the PC CPU to the no protocol send buffer memory area (hereafter referred to as the send area).

(1) Send area

Write the send data number and the send data in the send area as shown below.

The send area is assigned 0_H to $7F_H$ (for the RS-232C) or 100_H to $17F_H$ (for the RS-422) as default values.

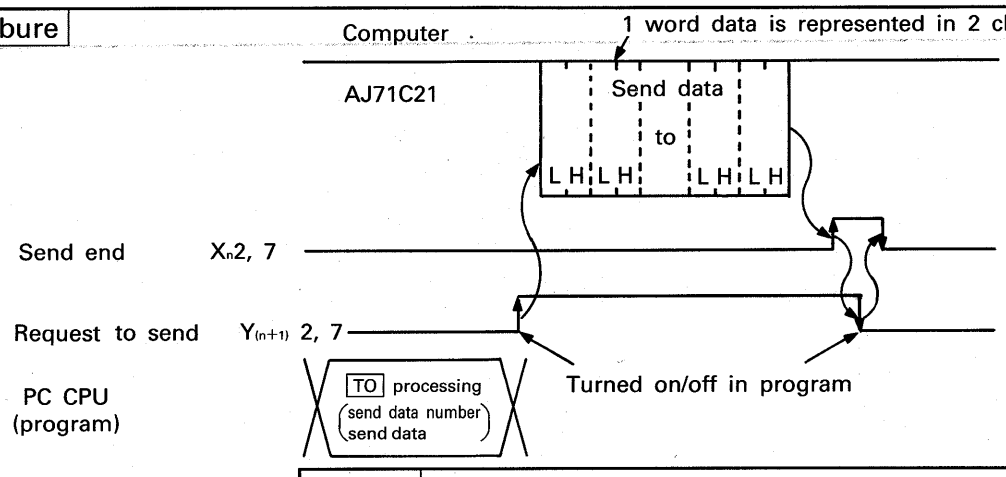
The send area can be changed according to the specific data send purpose and the external equipment specifications (for details on the changing method, refer to Section 6.1.8).



(2) Send procedure

The procedure for outputting the data stored in the send area to the external equipment is described below.

Procebure



POINT

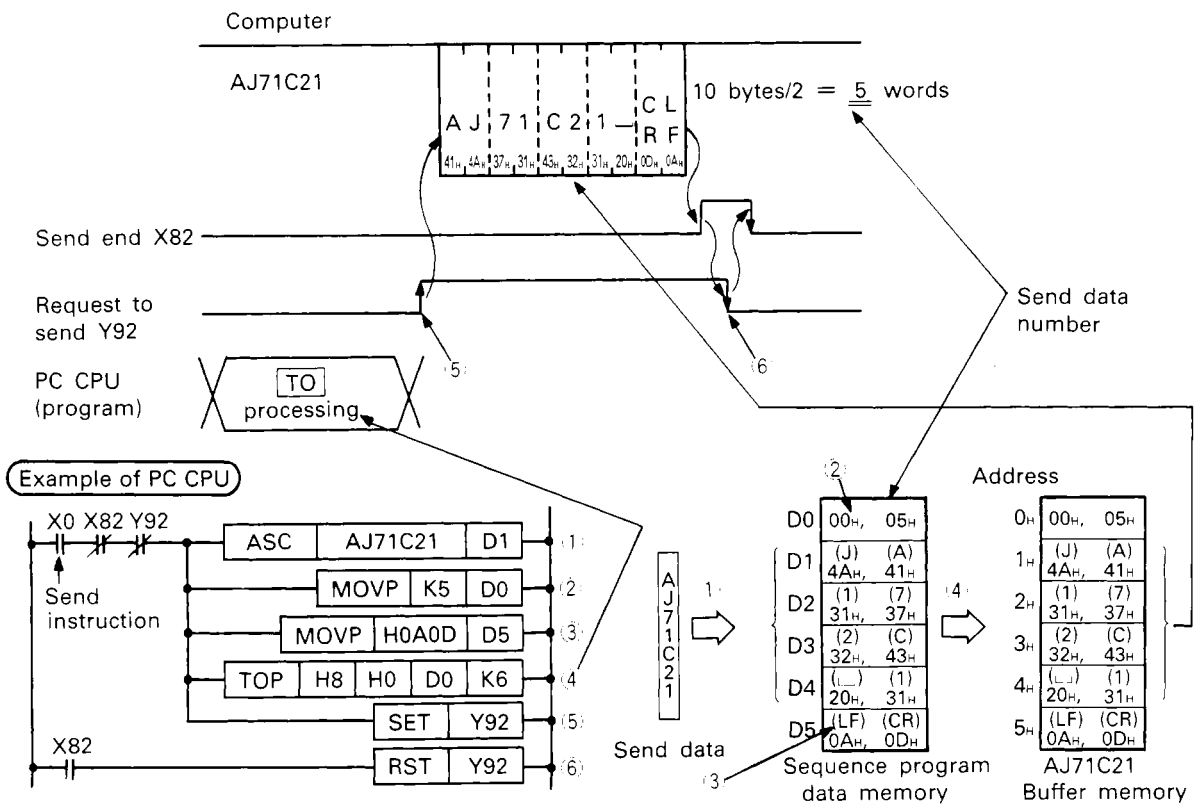
(1) When the send data number is greater than the send area or when the send data is "0", a no protocol send data number error occurs. As a result, the "1" that represents send error information is written into an upper bit (b14/b15) in the specific-use area 200_H (error LED display area) (for details, refer to Section 6.1.5).

(2) The send data number stored at the head address cannot be sent as data.

(3) Example of send program

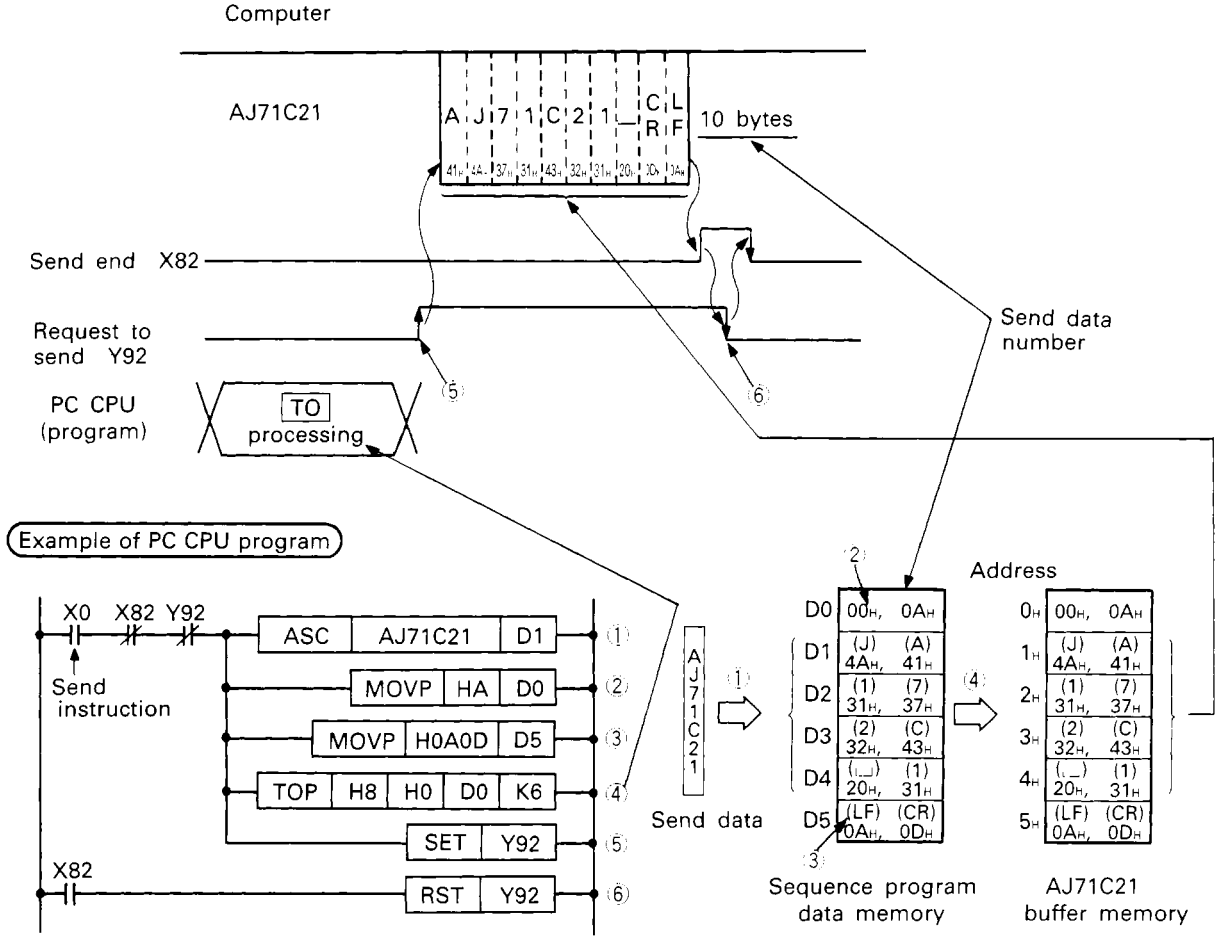
Example 1: In word units (buffer memory assignment with default values)

To send or output "AJ71C21" CR, LF from the PC CPU to the external equipment (AJ71C21 I/0 address: 80 to 9F; I/F used: RS-232C).



Example 2: In byte units (buffer memory assignment with default values)

To send or output "AJ71C21" CR, LF from the PC CPU to the external equipment (AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C).



POINT

Even when the send data is specified in byte units, the TO instruction from the PC CPU is represented in word units.
Therefore, the send data number differs from the TO instruction specified data number.

6.1.13 Receive in no protocol mode (external equipment → AJ71C21)

The "receive" occurs when the data received from the external equipment is stored in the buffer memory area for no protocol receive (hereafter referred to as the receive area) and the PC CPU reads it with the FROM instruction.

(1) Receive area

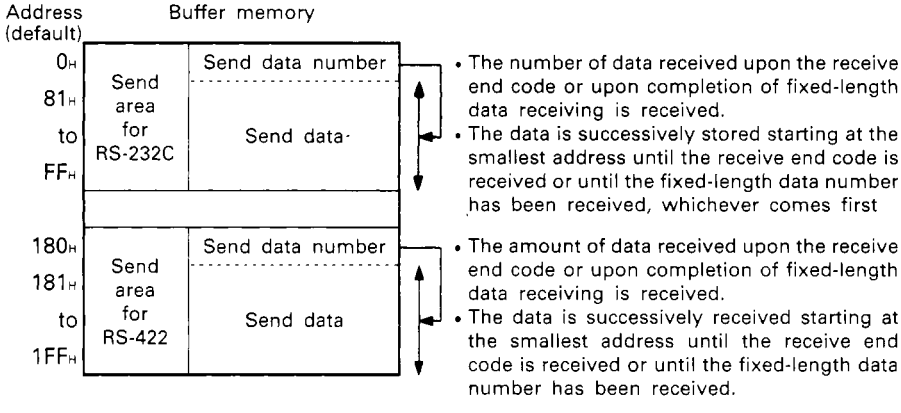
The receive area stores the receive data number and receive data.

The receive area is assigned 80_H to FF_H (for the RS-232C) or 180_H to $1FF_H$ (for the RS-422) as default values.

The receive area can be changed according to the specific data transmission purpose and the external equipment specifications (for details on the changing method, refer to Section 6.1.9).

For example, when the data received at one time exceeds the receive area (127 words as default), it can be divided so as to be appropriate for proper receiving.

It is recommended that the setting be made so that (receive area)>(receive data number) (for an example of the receive program, refer to remarks below).



(2) Receiving method

To finish receiving data, two methods are available: receiving the end code and receiving the preset data number (fixed length).

(a) Receiving end code

One round of data receiving is completed when the AJ71C21 receives the data specified in the end code.

The preset default is CR, LF ($0D0A_H$). However, it can be changed over the range 0000_H to $00FF_H$ (for details on the changing method, refer to Section 6.1.11).

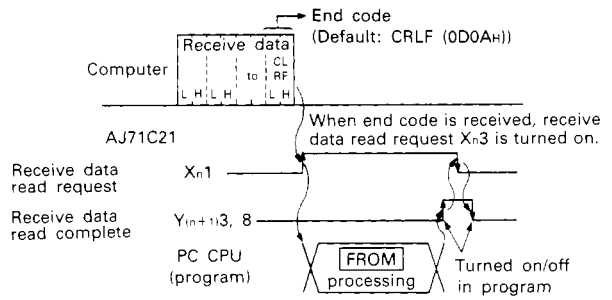
(b) Receiving fixed length data

One round of data receiving is completed when the AJ71C21 receives the preset data number.

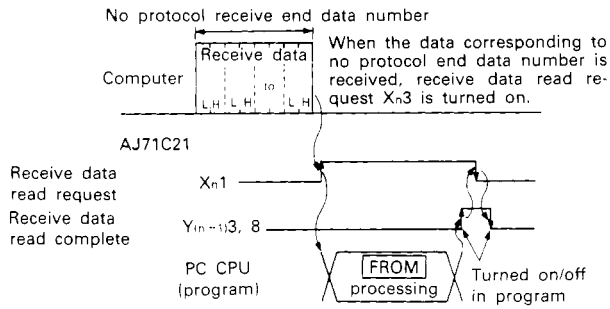
In fixed-length data receiving, all data ranging from 00_H to FF_H can be received since there is no need of setting specific codes, such as end code (for details on the setting method, refer to Section 6.1.10).

(3) Receiving procedure

Receive end with end code



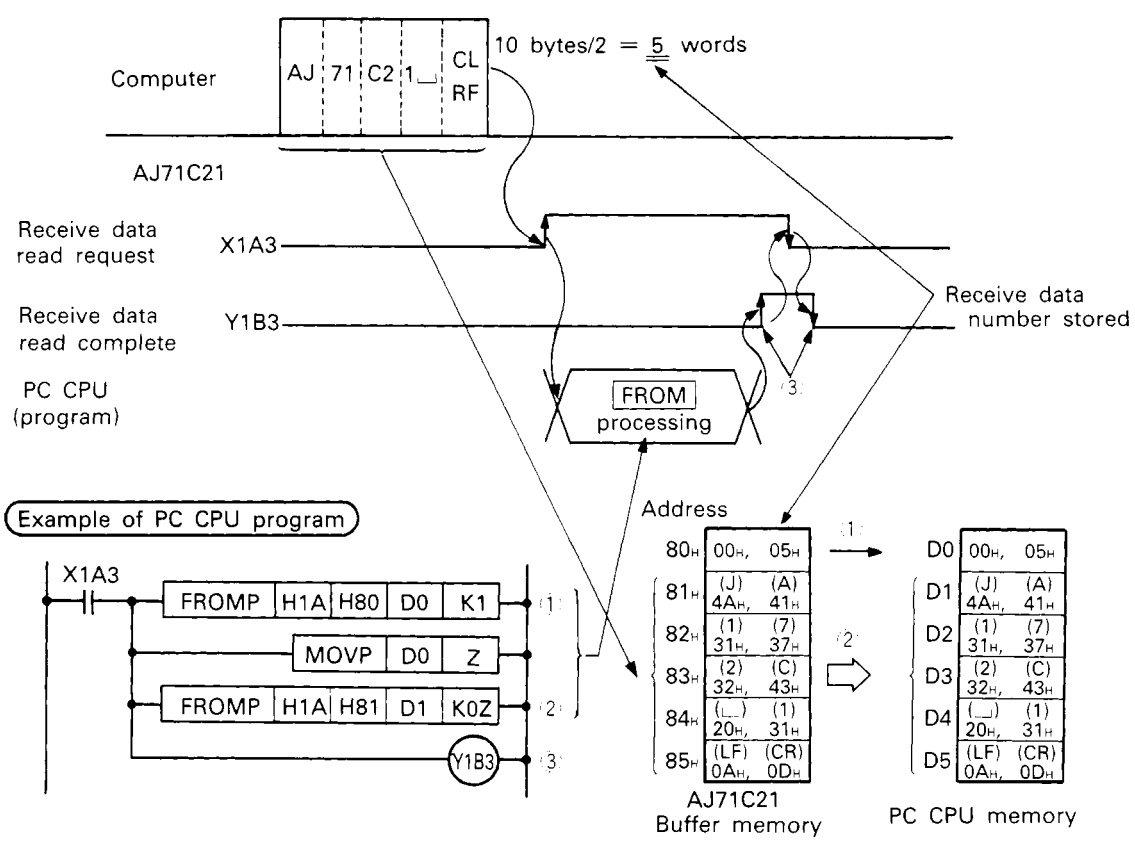
Receive end with fixed length



(4) Example of receive program

Example 1: In word units and with end code (buffer memory assignment with default values)

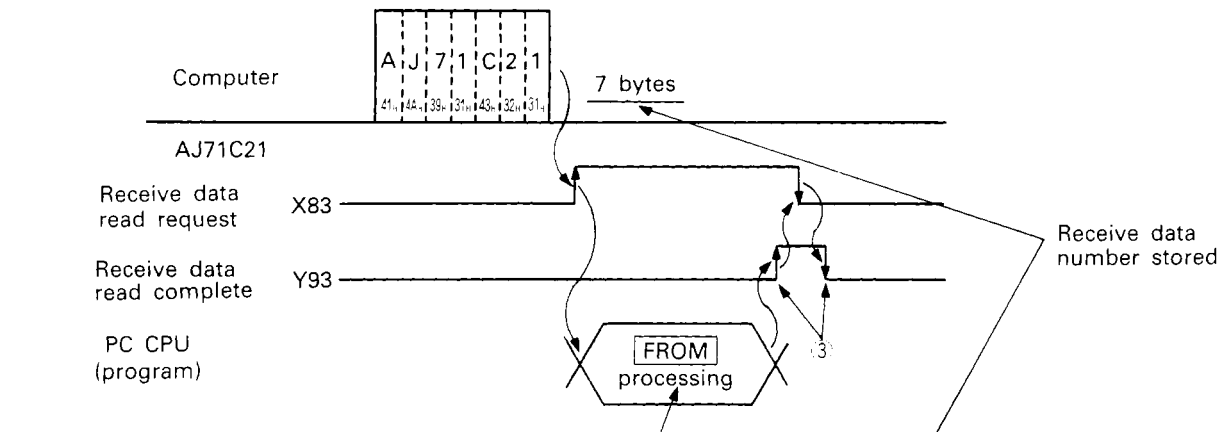
To receive "AJ71C21" CR, LF from the external equipment and store it in PC CPU at D0 through D5 (AJ71C21 I/O address: 1A0 through 1BF; I/F used: RS-232C)



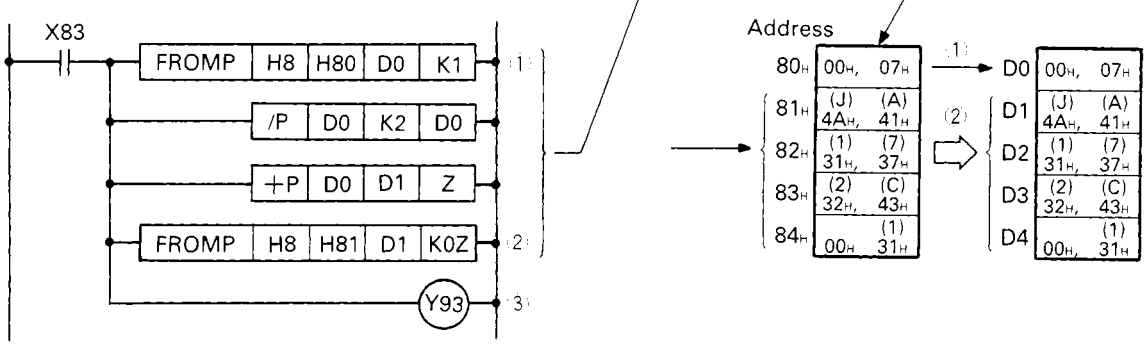
IB (NA) 66198-A

Example 2: In byte units and with fixed length
(buffer memory assignment with default values)

To receive "AJ71C21" from the external equipment and store it in the PC CPU at D0 through D4 (AJ71C21 I/O address: 80 to 9F; I/F used: RS-232C)



Example of PC CPU program



POINT

- **Even when the transmission data is specified in byte units, the FROM instruction from the PC CPU is denoted in word units. Therefore, it is necessary to change the receive data number to the buffer memory point number (in word units).**
  In the example above, 7 bytes is 7 ÷ 2 = 3.5 or 4 words.
- **When an odd byte is received, the upper 8 bits read with the FROM instruction becomes 00H.**

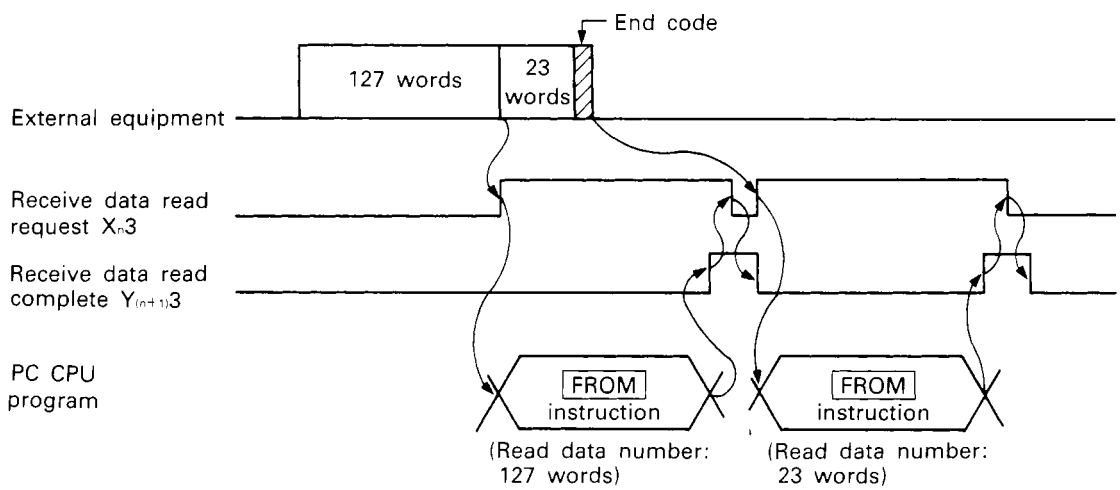
IB (NA) 66198-A

REMARKS

Processing of receive data length > no protocol receive buffer memory length

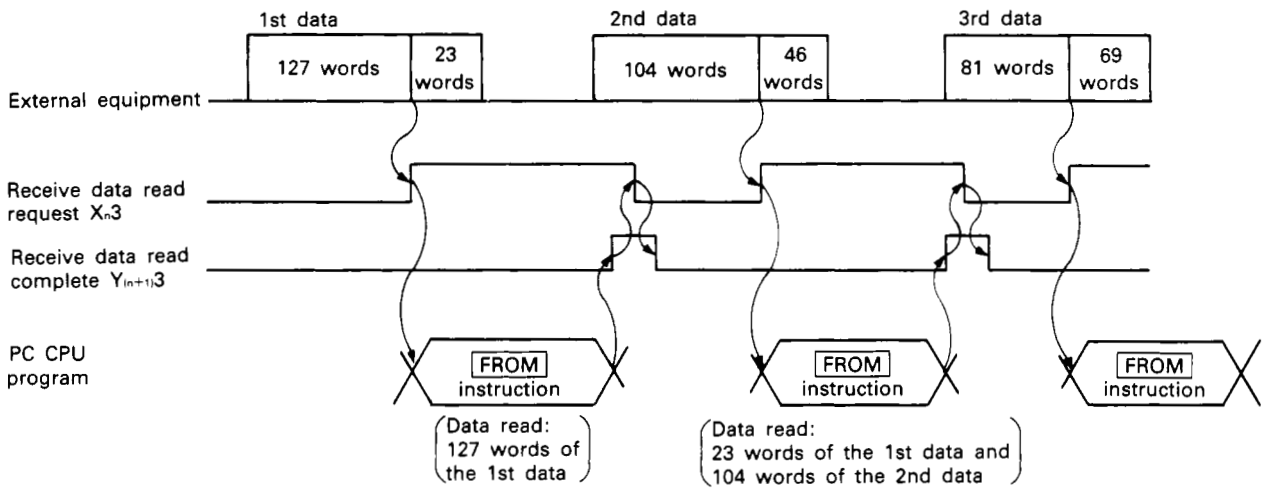
(1) Receiving with end code
When there is too much data to be stored in the receive area received by the AJ71C21, the receive data read request signal Xn3 is turned on.
When the PC CPU turns on the receive data read complete signal $Y_{(n+1)}3$, reading the remaining data becomes possible.
This procedure repeats itself until the end code is received.
Set the receive area so that the receive data length < no protocol receive buffer memory length.

Example: To receive the 150-word data when the receive area has 80_H through FF_H addresses (default values for the RC-232C of the I/F in use).



(2) Receive with fixed length
With the receive end data number set so that it exceeds the receive area, the no protocol receive buffer area length (default, 127 words) is processed as the receive end data number.
Set the receive area so that receive data length is smaller than no protocol buffer memory length.

Example: To receive 150-word data when the receive area has 80_H through FF_H addresses (default values for the RS-232C of the I/F in use).



IB (NA) 66198-A

(5) Receive buffer memory clear

If an error is caused by malfunctioning external equipment or other factors while data is being received from such equipment in the no protocol mode, the data already received may contain errors. For error recovery, the AJ71C21 can be initialized by clearing all received data.

(a) Error detection

The following methods are available for detecting errors that can occur during receiving.

1) Error LED display area read

For error detection purposes, the PC CPU reads the error LED ON/OFF status which is stored as transmission control information at address 200_H in the buffer memory.

2) PC input signal

The ready signal and other signals from the external equipment are connected to the PC CPU so that any error is detected by checking the signal ON/OFF status.

(b) Receive data clear

1) Data clear range

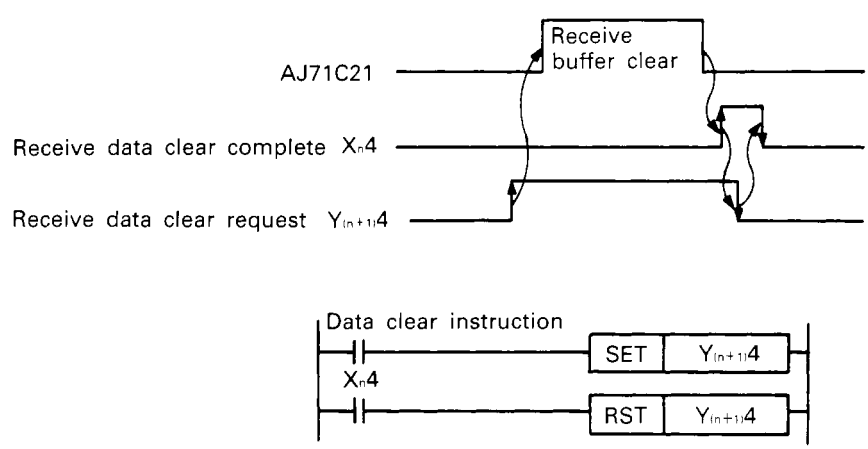
The AJ71C21 clears all data already received and the no protocol receive memory area is initialized.

2) Receive data clearing method

The receive data can be cleared by turning on $Y_{(n+1)}4$/$Y_{(n+1)}9$ with the sequence program.

Upon completion of receive data clear, the AJ71C21 turns on X_n4/X_n9.

Example of receive data clear program (I/F in use: RS-232C)



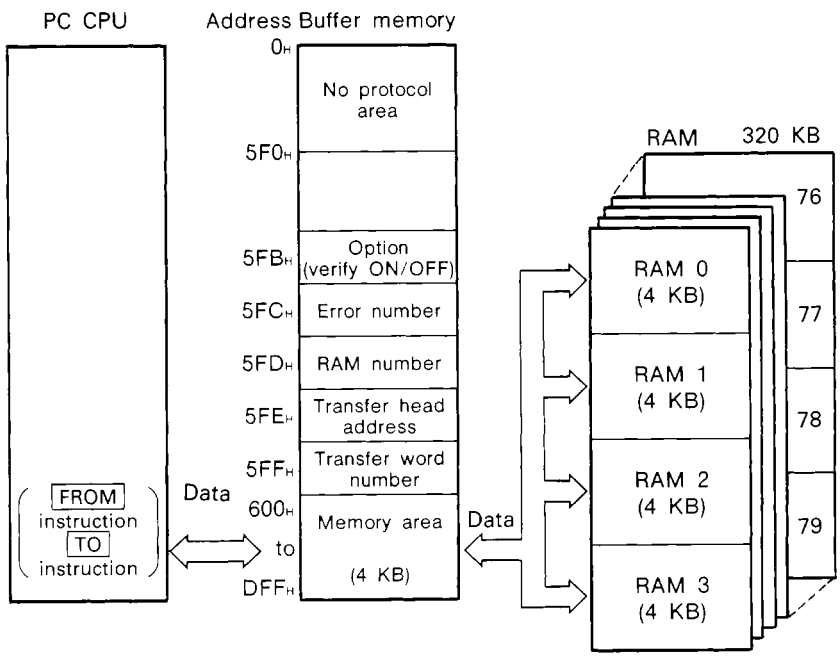
IB (NA) 66798-A

6.2 Data Read/Write (Only for the AJ71C21-S1)

6.2.1 Data read/write

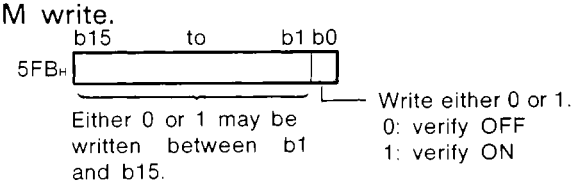
The AJ71C21-S1 incorporates a 320K byte RAM which can hold a great deal of data. The PC CPU can write data to read data from this memory space which is used as an external auxiliary register for the PC CPU.
When connected to the GPP, the RAM permits the memory contents to be stored on a floppy disk.

Access (write/read) from the PC CPU to the AJ71C21-S1 RAM memory is gained in 4K byte units via the buffer memory by switching the bank (RAM number specification).



The memory is delimited in 4K byte units and each delimited memory is called RAM. The RAMs are numbered 0 to 79.
The memory is accessed in 4K byte units and no access is gained when any RAM number is skipped.
The data stored in the buffer memory is written at the same address as that in the RAM with the specified number. The data stored in the memory is read at the same address in the buffer memory by specifying the RAM number and the head address.

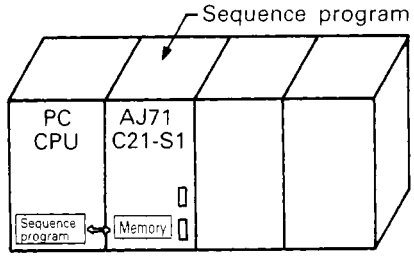
The buffer memory option area is used to specify the verify ON/OFF between the buffer memory and the RAM at the time of RAM write.



In the event of the occurrence of a verify error, store error No. 5 at 5FCH in the buffer memory area. After removing the cause of the error, clear the error number and rewrite.

IB (NA) 66198-A

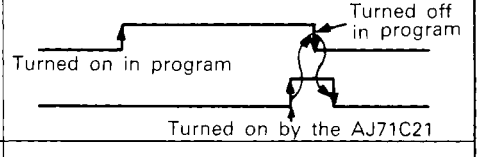
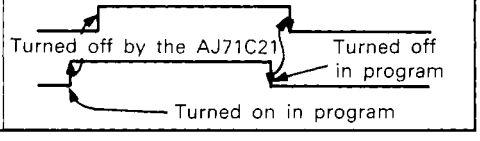
For the AJ71C21 hardware setting, set the I/F mode setting switch on the front panel to the "0" position and set the inner program mode setting switch No. 1 to the OFF position (sequence program mode).

Switch Setting		System Configuration
Mode setting	Program mode setting	
		

Only applicable to the AJ71C21-S1

6.2.2 I/O handshake signals

The term "I/O handshake signals" refers, among other things, to the signal which is used to output data from the PC CPU to the memory or by which the PC CPU becomes capable of reading the data arriving from the memory. This signal is indispensable when the PC CPU is used to write data to and read data from the RAM memory space.
The I/O signals for handshake are detailed below.

	Signal		Timing
PC CPU ↓ RAM	Y(n+1) C Xn C	(request to write) (write complete)	
RAM ↓ PC CPU	Xn D Y(n+1) D	(request to read) (read complete)	

IB (NA) 66198-A

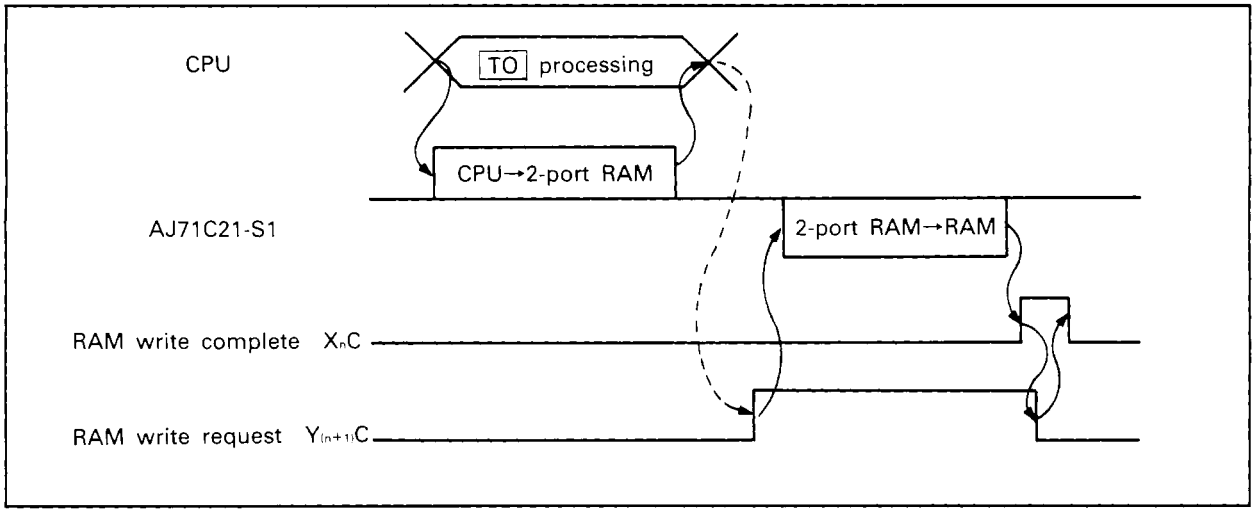
6.2.3 RAM write

This section describes the procedure for writing data from the PC CPU to the AJ71C21-S1 built-in RAM.

(1) The RAM number, transfer head address, transfer word number, data required to set data verify ON/OFF during write, and other data is read from the user's program for storage in the specified buffer memory.

Buffer Memory Address	Set Data	Data Set
5FB$_H$	Verify ON/OFF	0: verify OFF; 1: verify ON
5FD$_H$	RAM number	0 to 79
5FE$_H$	Write head address	600$_H$ to DFF$_H$
5FF$_H$	Write word number	1 to 2048 words

(2) Write procedure

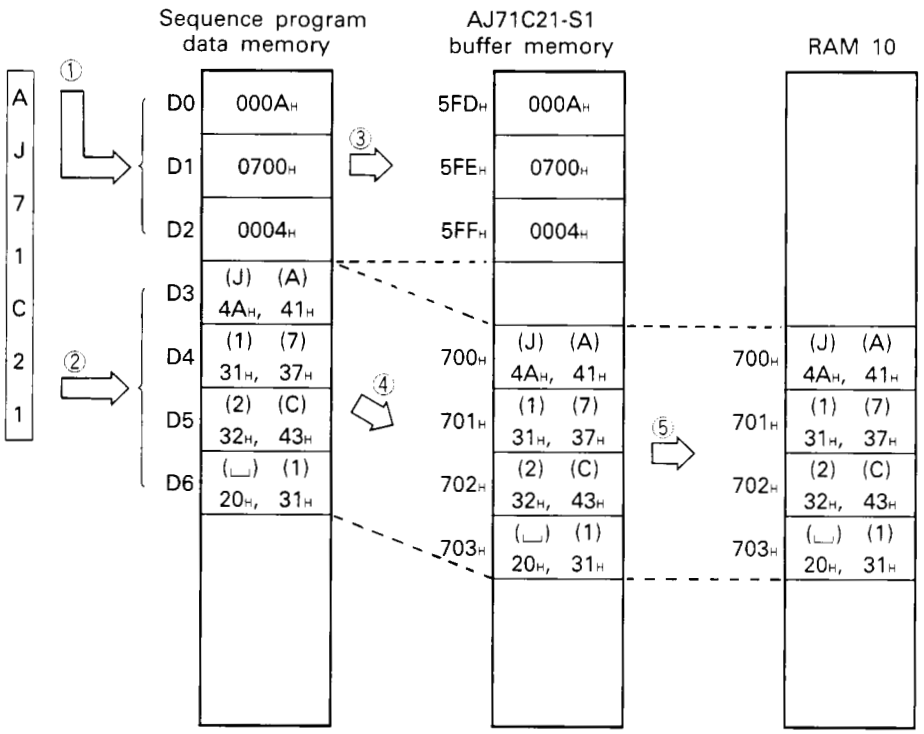


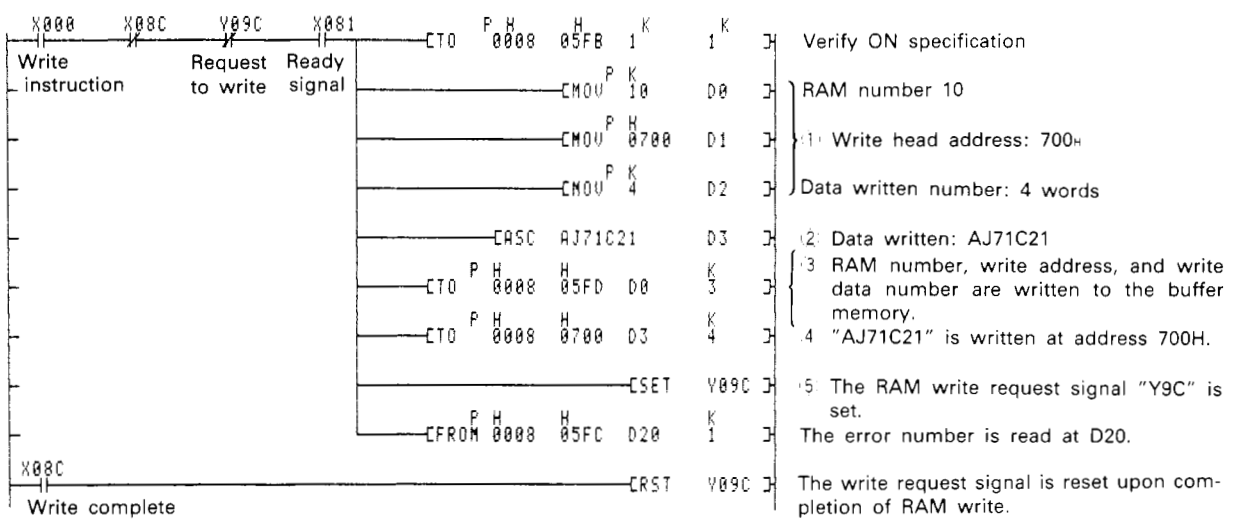
POINT

The RAM can be checked for abnormality and the RAM memory can be initialized by checking the RAM. For details on the RAM check, refer to Section 4.5.2.

(3) Example of write program

The "AJ71C21" ASCII data is written at addresses starting at 700_H in the memory RAM No.10. In the event of an error, the error number is read at D20 (AJ71C21 I/O addresses: 80 to 9F).





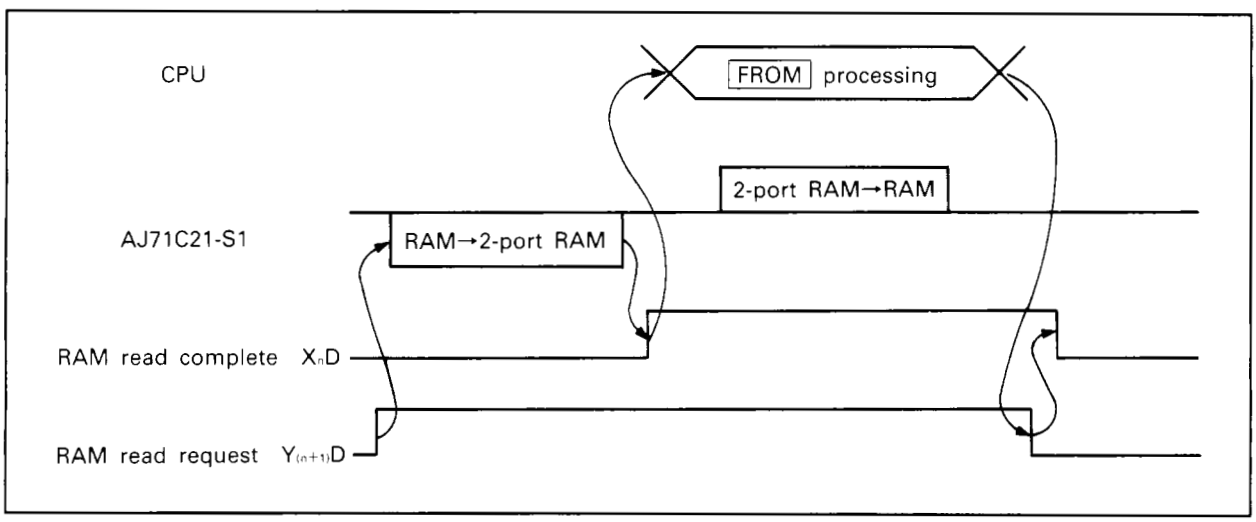
6.2.4 RAM read

This section describes the case when the data stored in the AJ71C21-S1 built-in RAM is read to the PC CPU.

(1) Memory data

Buffer Memory Address	Item	Data
5FD$_H$	RAM number	0 to 79
5FE$_H$	Stored data head address	600$_H$ to DFF$_H$
5FF$_H$	Read word number	1 to 2048 words
600$_H$ to DFF$_H$	Stored data area	

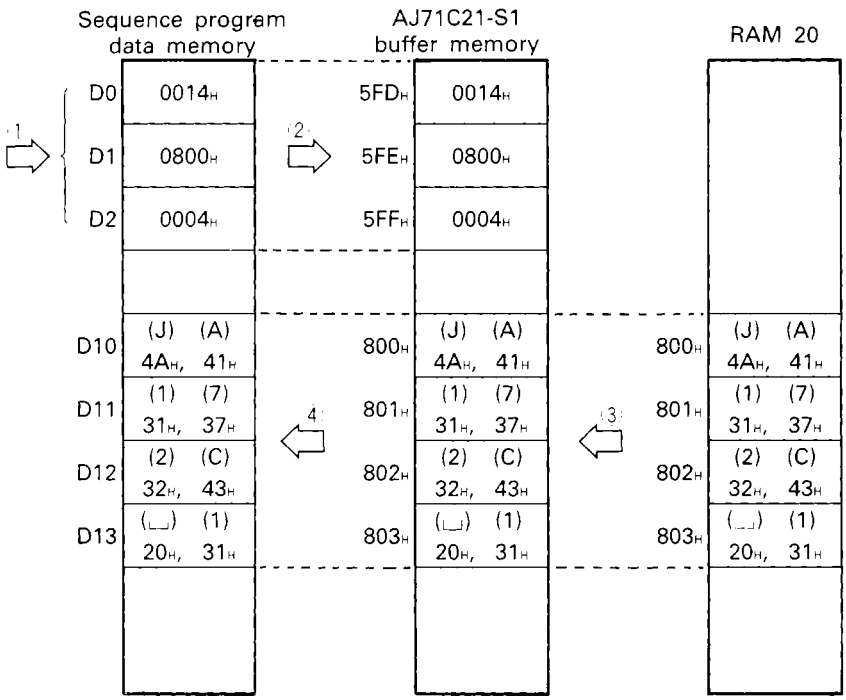
(2) Read procedure

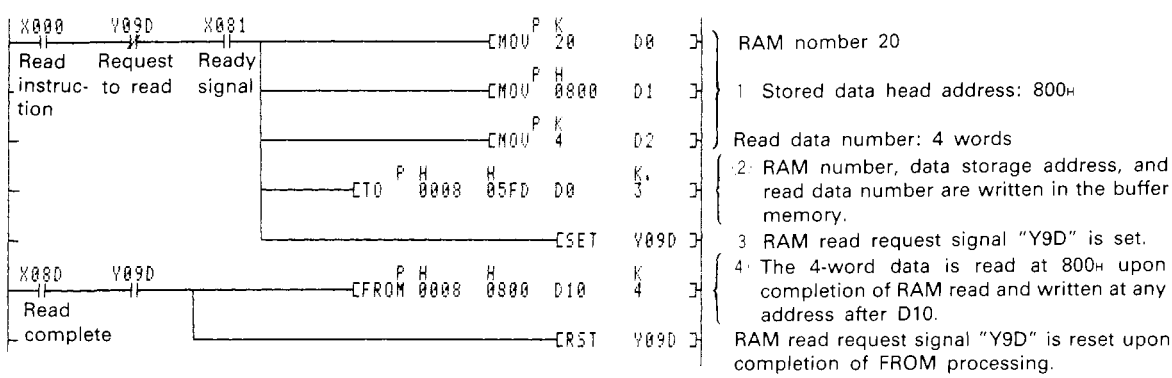


The RAM read request signal $Y_{(n+1)}D$ is turned on and off by the sequence program.

(3) Example of read program

The "AJ71C21" ASCII data is written at addresses starting at 700H in the memory RAM No.10. In the event of error occurrence, the error number is read at D20 (AJ71C21 I/O addresses: 80 to 9F).

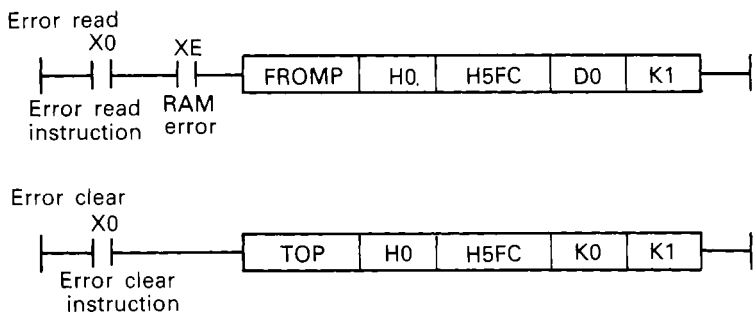




IB (NA) 66198-A

6.2.5 RAM error read and clear

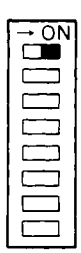
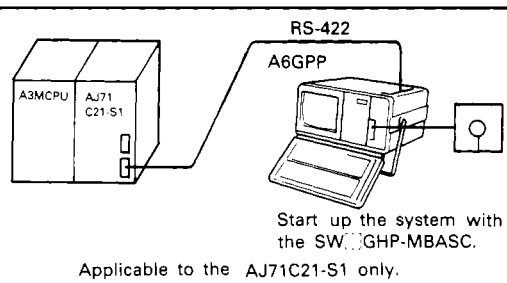
If an error occurs while data is being written to or read from the RAM, the X_nE (RAM error) signal is turned on and the error number is stored in the buffer memory (at $5FC_H$).
"0" is written with the TO instruction. Writing "0" turns off X_nE.
Next, the error definition is read. An example of the error clear program is given below (AJ71C21 I/O addresses: 0 to 1F).



6.2.6 Memory data backup

The AJ71C21-S1 memory remains backed-up during power failure. It can also be stored on a floppy disk when the GPP is connected.

(1) Connection between AJ71C21-S1 and GPP
Set the I/F mode setting switch on the AJ71C21-S1 front panel to the "3" position. Set the inner program mode setting switch to the OFF (sequence program mode) position.
Connect the AJ71C21-S1 with the GPP using the AC30R4 cable.

Switch Setting		System Configuration
Mode setting	Program mode setting	
		

(2) The following operations are performed via the GPP.
For details on operation, refer to the A3M-BASIC Type SW0GHP-MBASC Operating Manual.
Read: The data stored on a floppy disk is read to the AJ71C21-S1.
Write: The AJ71C21-S1 memory data is written on the floppy disk.
Verify: The data stored on the floppy disk is checked against the memory data in the AJ71C21-S1.

(3) This operation does not apply to the AJ71C21 (without a built-in memory). If an attempt is made to perform the operation, an error indication appears on the GPP.

(4) In the backup mode (with the I/F mode setting switch set at "3"), the X_n1 (AJ71C21 ready signal) remains off.

POINT

Do not write data from the CPU to the AJ71C21-S1 RAM being accessed in the backup mode. If this precaution is not taken, the data in the RAM will be rewritten. Use care not to switch the power off during data access.
Follow the suggestions given below to prevent write in the RAM.
(1) Set the CPU to STOP.
(2) Effect interlocking so that the RAM write is done only when the AJ71C21-S1 ready signal (X_n1) is given.

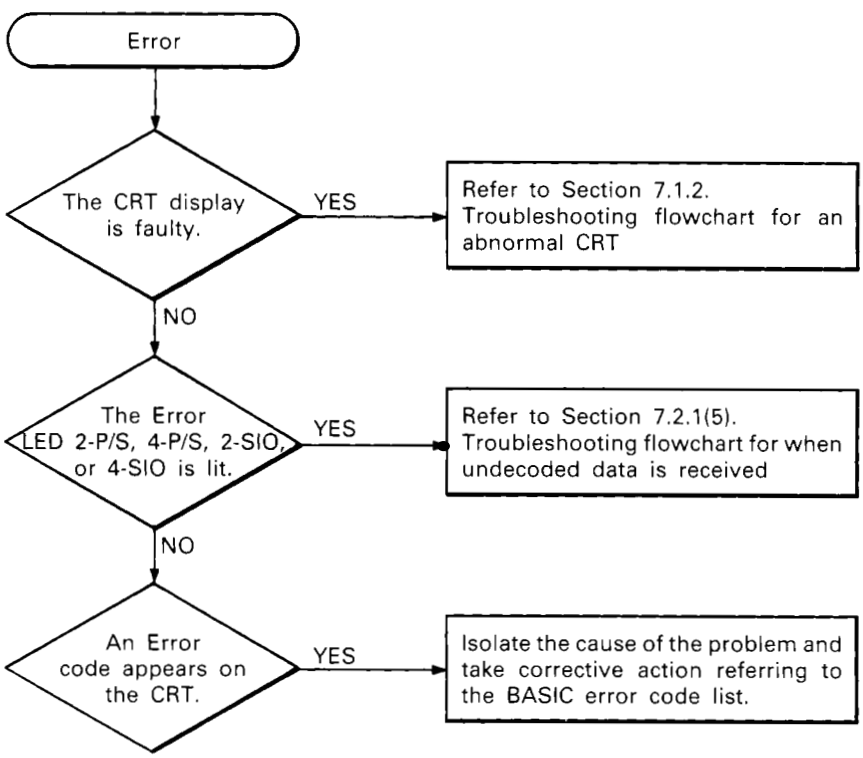
IB (NA) 66198-A

7. TROUBLESHOOTING

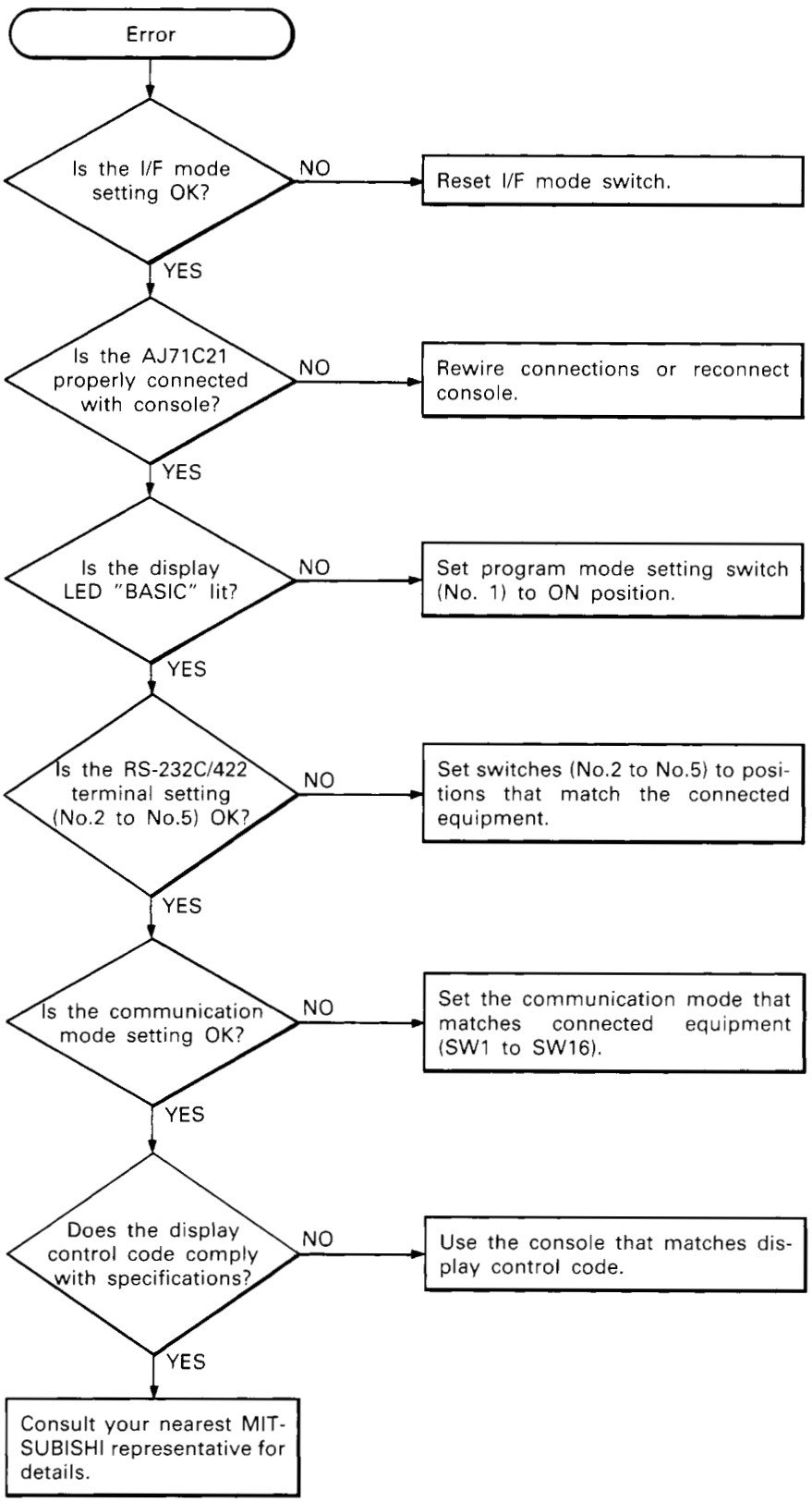
This section describes basic troubleshooting procedures for the AJ71C21.
For details on CPU troubleshooting and basics, refer to the CPU User's Manual and the A3M-MBASIC Type SW0GHP-MBASC Operating or Programming Manual, respectively.

7.1 Troubleshooting in BASIC Program Mode

7.1.1 Troubleshooting flowchart



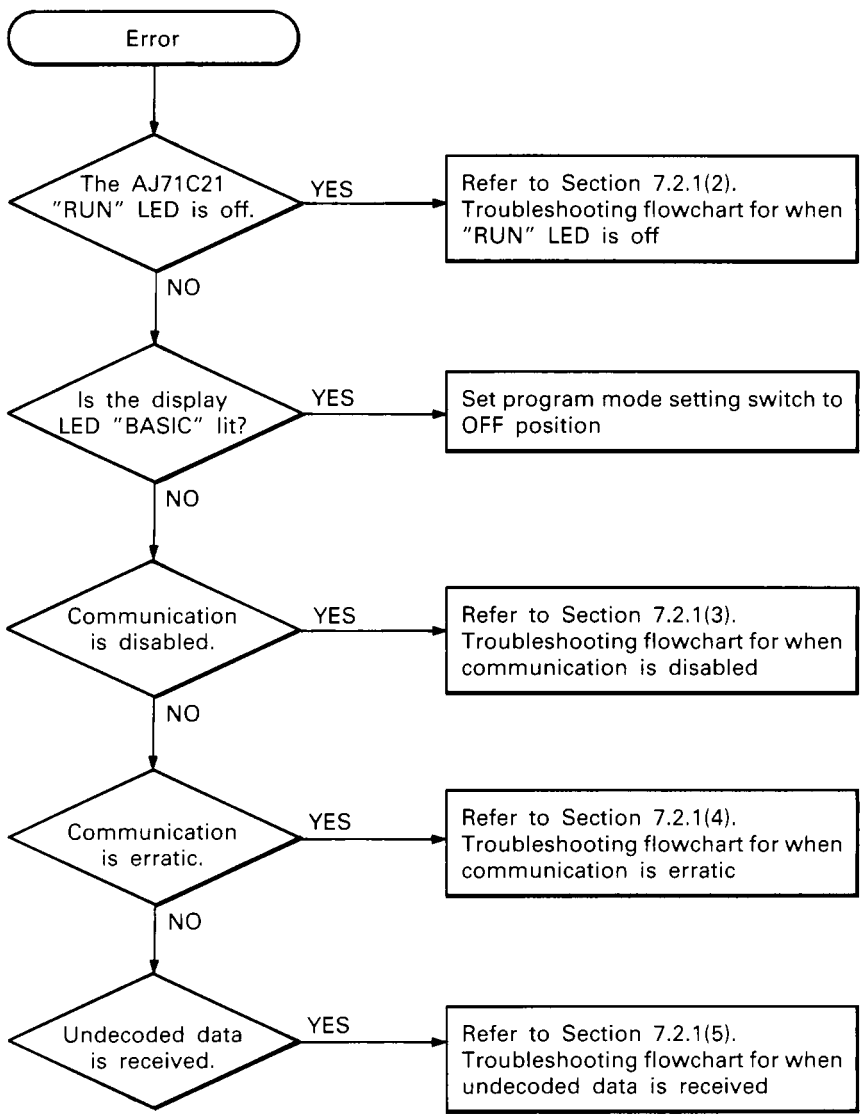
7.1.2 CRT display faulty



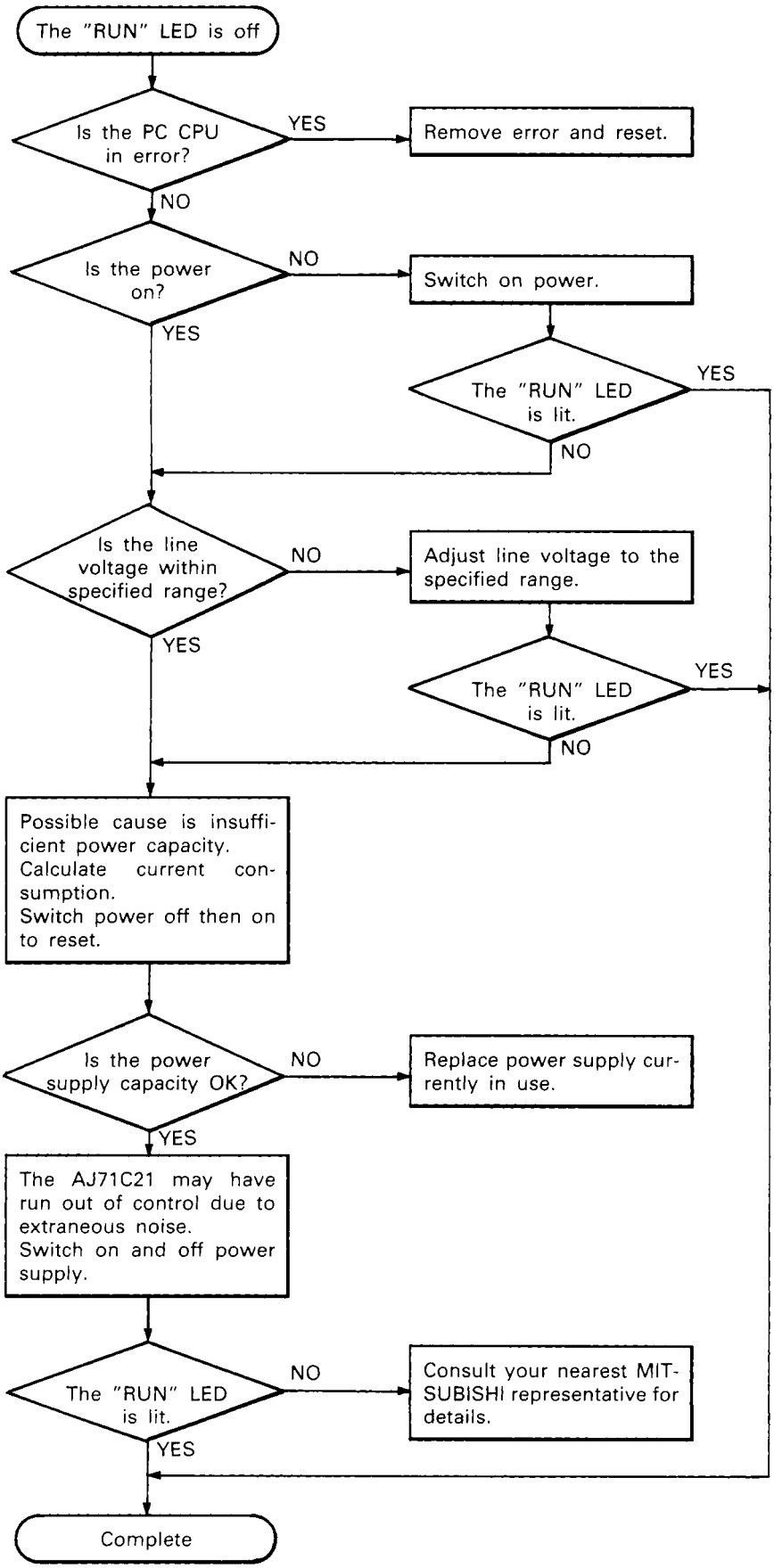
7.2 Troubleshooting in Sequence Program Mode

7.2.1 Troubleshooting during communication with external equipment in no protocol mode

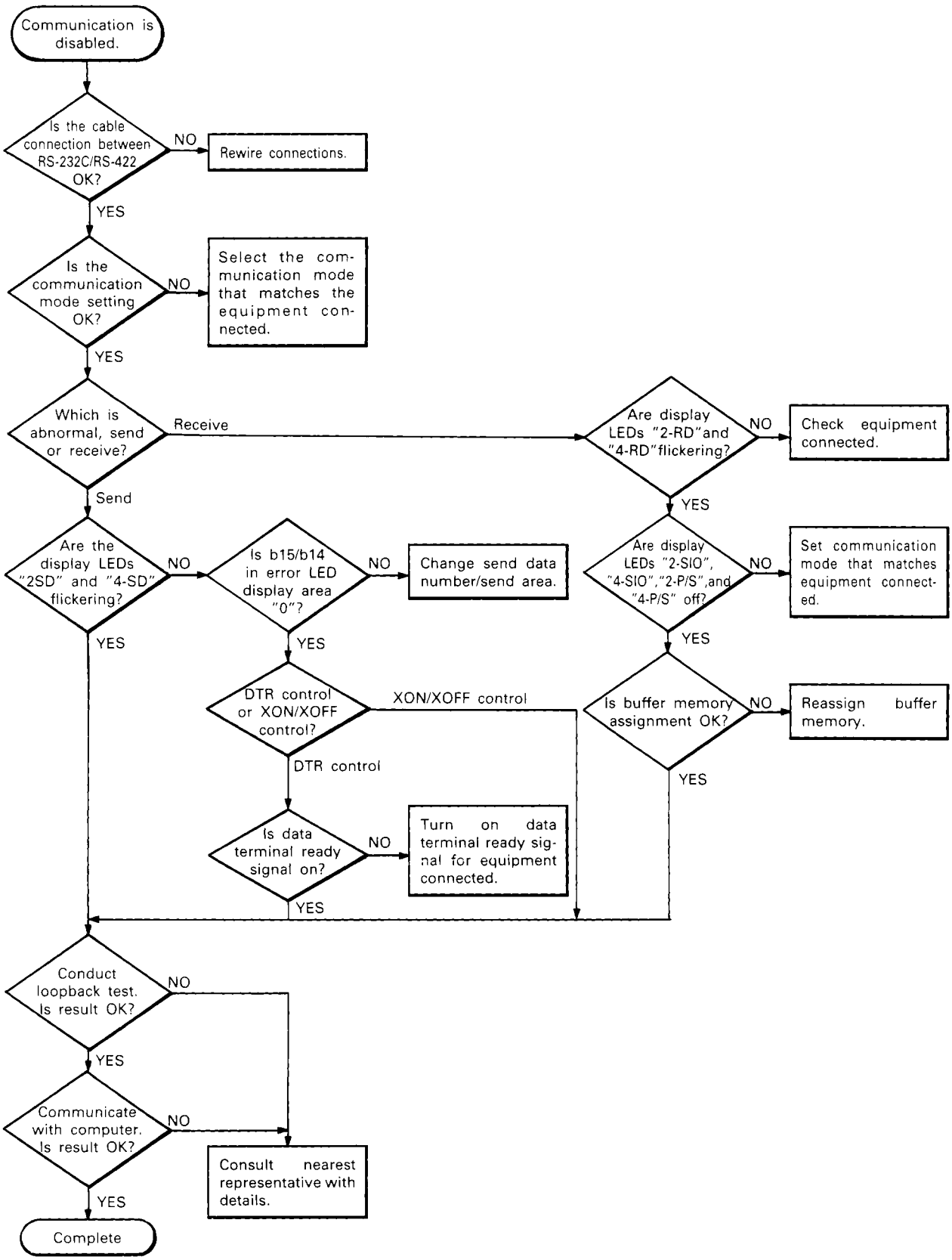
(1) Troubleshooting for flowchart



(2) Troubleshooting for flowchart when the "RUN" LED is off

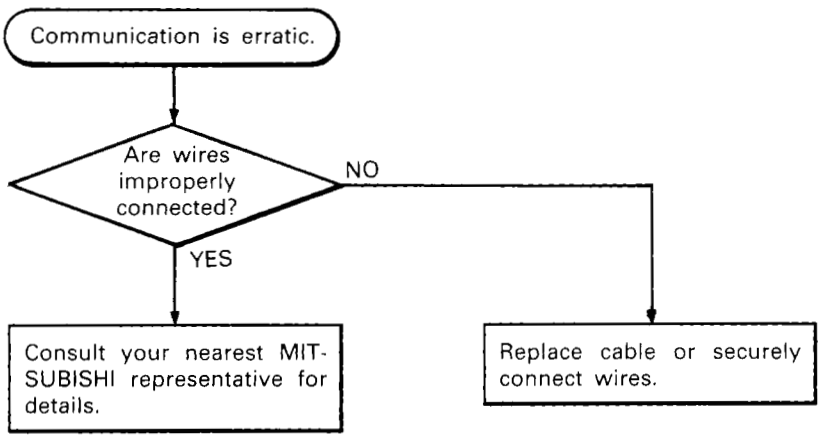


(3) Troubleshooting for flowchart when communication is disabled



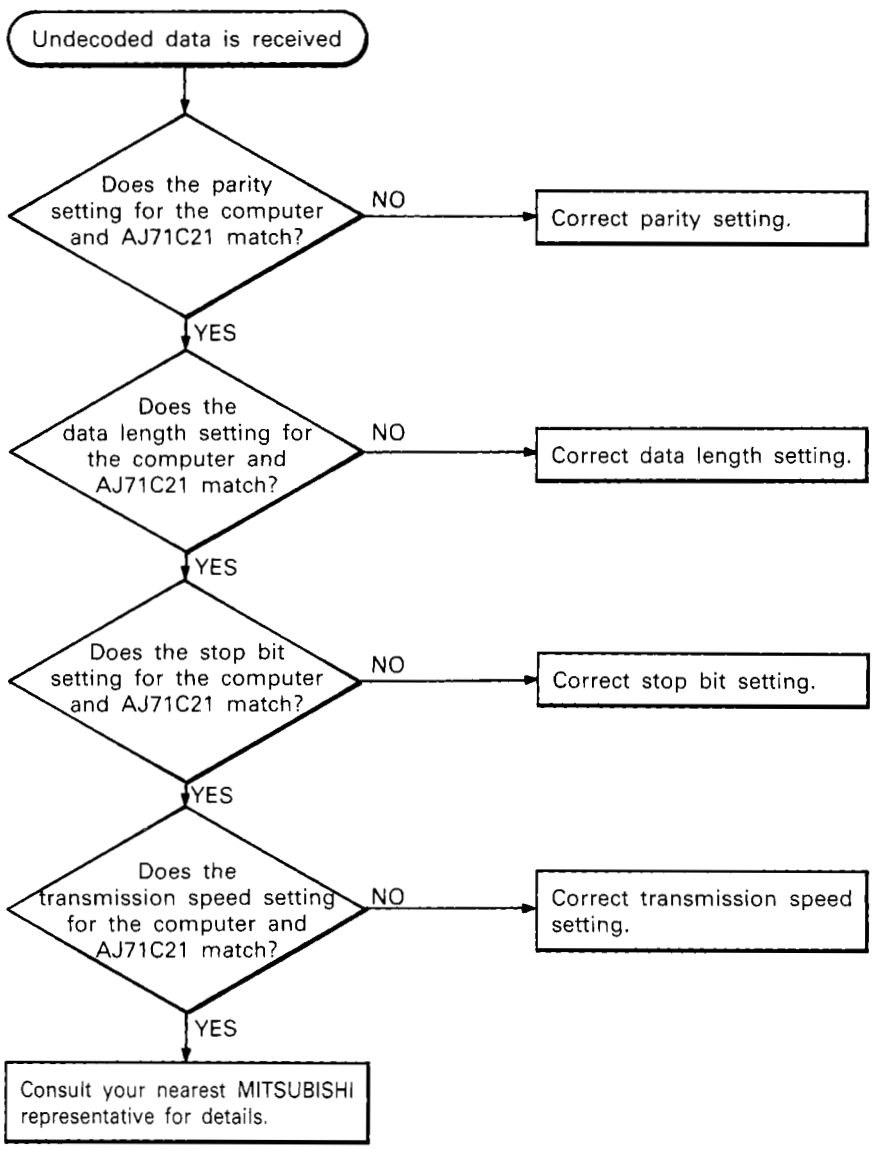
IB-NA 66198-A

(4) Troubleshooting flowchart for when communication is erratic



(5) Troubleshooting for flowchart when undecoded data is received

The following is a flowchart used when the AJ71C21 receives undecoded data which is not found in the control code received from the computer.



7.2.2 RAM write/read error

When an error occurs while data is being written to or read from the RAM, the error number is stored at $5FC_H$ in the buffer memory. In that event, read the error number, isolate the cause of the problem, and take corrective action.
For details on the method for reading the error number and clearing the error, refer to Section 6.2.5.

Error Number	Error Definition	Description
1	RAM number error	A number other than 0 to 79 has been set. The AJ71C21 has been accessed.
2	Transfer head address error	A head address has been set to other than 600_H to DFF_H.
3	Transfer word number error	A number other than 1 to 2048 has been set.
4	Transfer area error	The head address + transfer word number −1 exceeds DFF_H.
5	Verify error	Unmatched data is found upon verify.
6	RAM access error	The RAM cannot be accessed during data write or read.

Table 7.1 List of RAM Errors

APPENDICES

APPENDIX 1 Comparison in Function between the AJ71C21 and the AJ71C24-S3 (Computer Link Module)

Function \ Module		AJ71C21		AJ71C21-S1		AJ71C24 -S3
		BASIC program mode	Sequence program mode	BASIC program mode	Sequence program mode	
BASIC	BASIC	○	×	○	×	×
Com-muni-cation	Computer link with dedicated protocol	×	×	×	×	○
	No protocol computer link	×	○	×	○	○
Memory	Data read from and write to memory	×	×	×	○	×

APP

IB (NA) 66198-A

APPENDIX 2 ASCII Code Table

Character codes used for the computer link are listed below (7-bit codes).

LSD \ MSD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	!!	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	/	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
A	1010	LF	SUB	*	:	J	Z	j	z
B	1011	VT	ESC	+	;	K	[	k	{
C	1100	FF	FS	,	<	L	\	l	|
D	1101	CR	GS	-	=	M	]	m	}
E	1110	SO	RS	.	>	N	↑	n	~
F	1111	SI	VS	/	?	O	←	o	DEL

APP

APPENDIX 3 Display Control Code List

When the VT-220 is set for the AJ71C21(S1) RS-232C/RS-422 terminal setting, the following display control code is obtained.

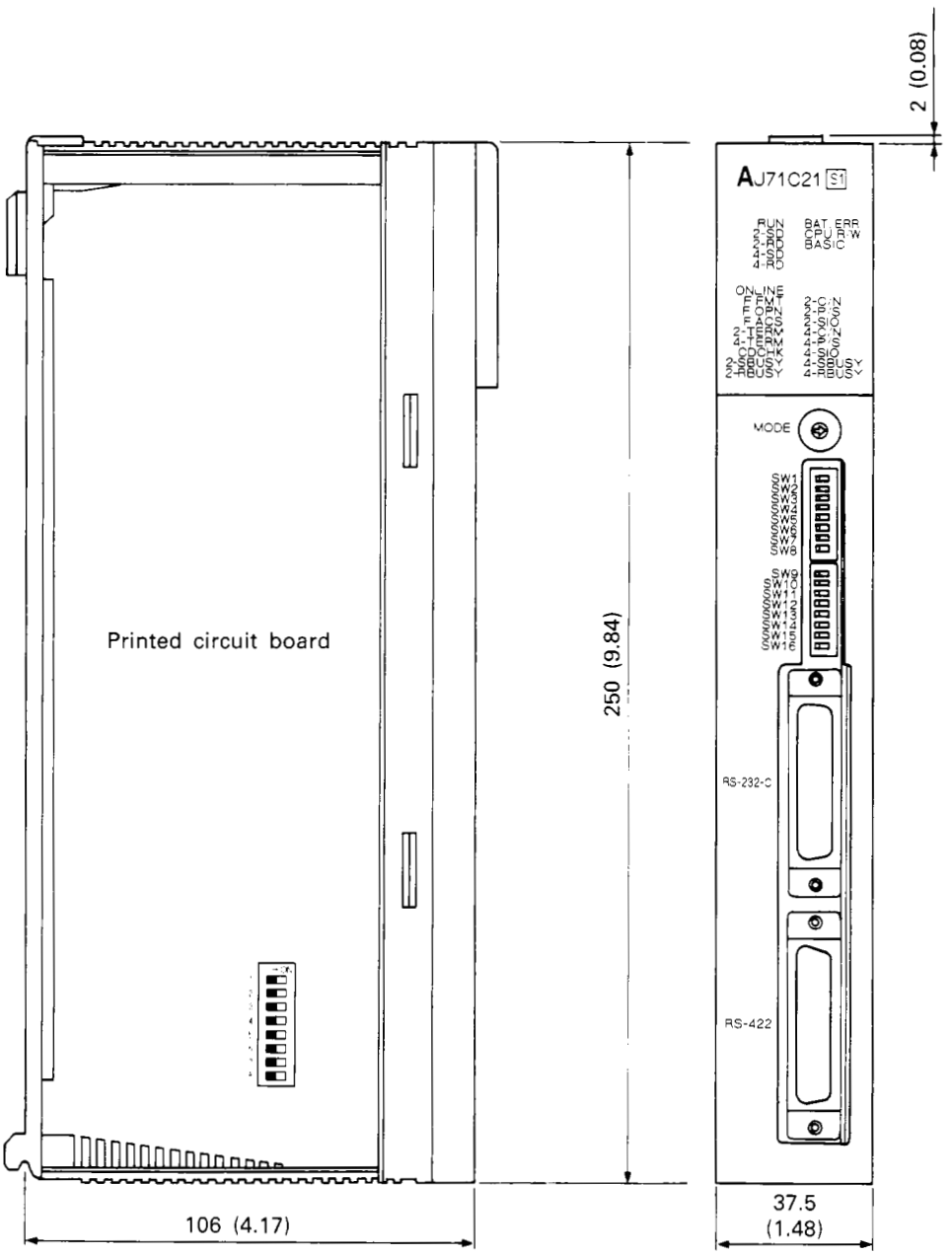
Function	Description	Code Used (ASCII) With VT-220	BASIC Instruction
Line feed	Carriage return	CR, LF code(0D$_H$,0A$_H$)	—
Screen clear	Total screen clear	ESC+[(5B$_H$)+2(32$_H$)+J(4A$_H$)	CLS
XON operation	Specification of transfer enable from external equipment	DC1 code(11$_H$)	—
XOFF operation	Specification of transfer disable from external equipment	DC3 code(13$_H$)	—
Escape operation	Escape sequence introducer	ESC code(1B$_H$)	—
Cursor control	Cursor backward	BS code(08$_H$)	—
	Cursor up	ESC+[(5B$_H$)+1(31$_H$)+A(41$_H$)	—
	Cursor down	ESC+[(5B$_H$)+1(31$_H$)+B(42$_H$)	—
	Cursor right	ESC+[(5B$_H$)+1(31$_H$)+D(43$_H$)	—
	Cursor left	ESC+[(5B$_H$)+1(31$_H$)+D(44$_H$)	—
Cursor addressing	Specification of cursor position at absolute	ESC +[(5B$_H$) +Line position specification+;(3B$_H$) +Column position specification+H(48$_H$)	LOCATE
Audible alarm	Bell rings	BEL code (07$_H$)	—

Display Control Code List

APP

IB (NA) 66198-A

APPENDIX 4 Dimensions



Unit: mm (inch)

APP

IB (NA) 66198 A

IMPORTANT

The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(1) Ground human body and work bench.

(2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your specific application.

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE: MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100 TELEX: J24532 CABLE MELCO TOKYO
NAGOYA WORKS : 1-14 , YADA-MINAMI 5 , HIGASHI-KU , NAGOYA , JAPAN

These products or technologies are subject to Japanese and/or COCOM strategic restrictions and diversion contrary thereto is prohibited.

IB (NA) 66198-A (8907) MEE Printed in Japan

Specifications subject to change without notice.